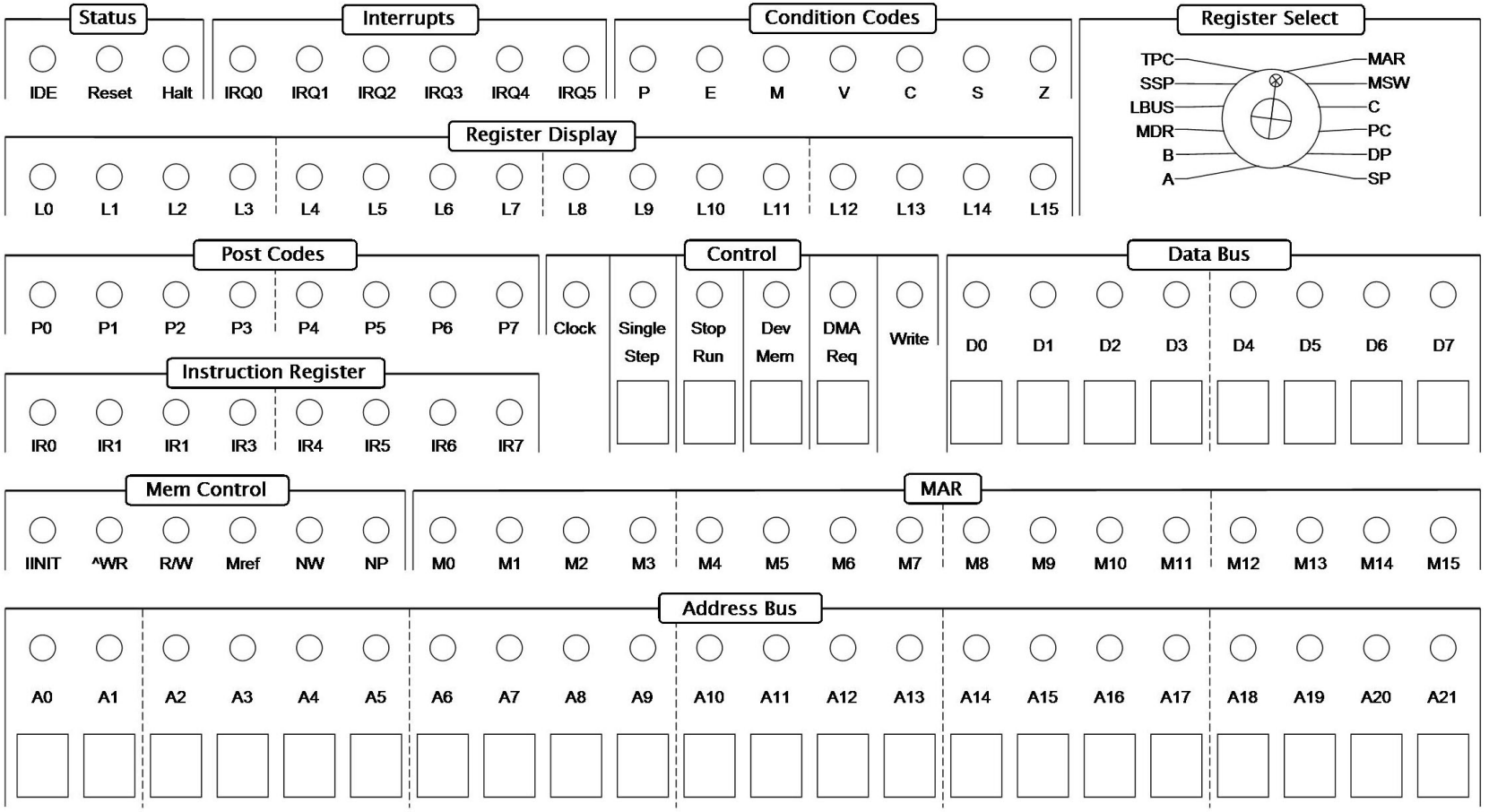
Updated 7/4/2016



Magic-1 Homebrew CPU

Bill Buzbee, Half Moon Bay, CA

Magic-1 Homebrew CPU

CPU: Custom design
Construction:
Wire-wrapped TTL
Clock speed: 3 Mhz
Memory: 4 MB
Architecture:
modified 1 address
Address bus:
22 bits + I/O space

Addressing modes:
Reg-Reg
Base + offset
Push, Pop
Registers:
General: A, B
Bases: SP, DP
Control: MSW, PTB
Special: PC, C

Hardware page table
Data bus: 8 bits
ALU width: 16 bits
Modes: supervisor & user
External interrupt lines: 6
IDE hard drive interface
Serial ports: 2
Real time clock
Full front panel

http://www.homebrewcpu.org

Magic-1 design & construction: Bill Buzbee

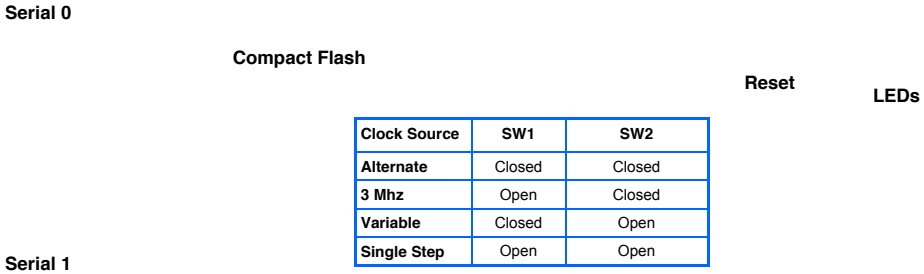
Enclosure and front panel: Alistair Roe

Design & debugging help, inspiration and encouragement:

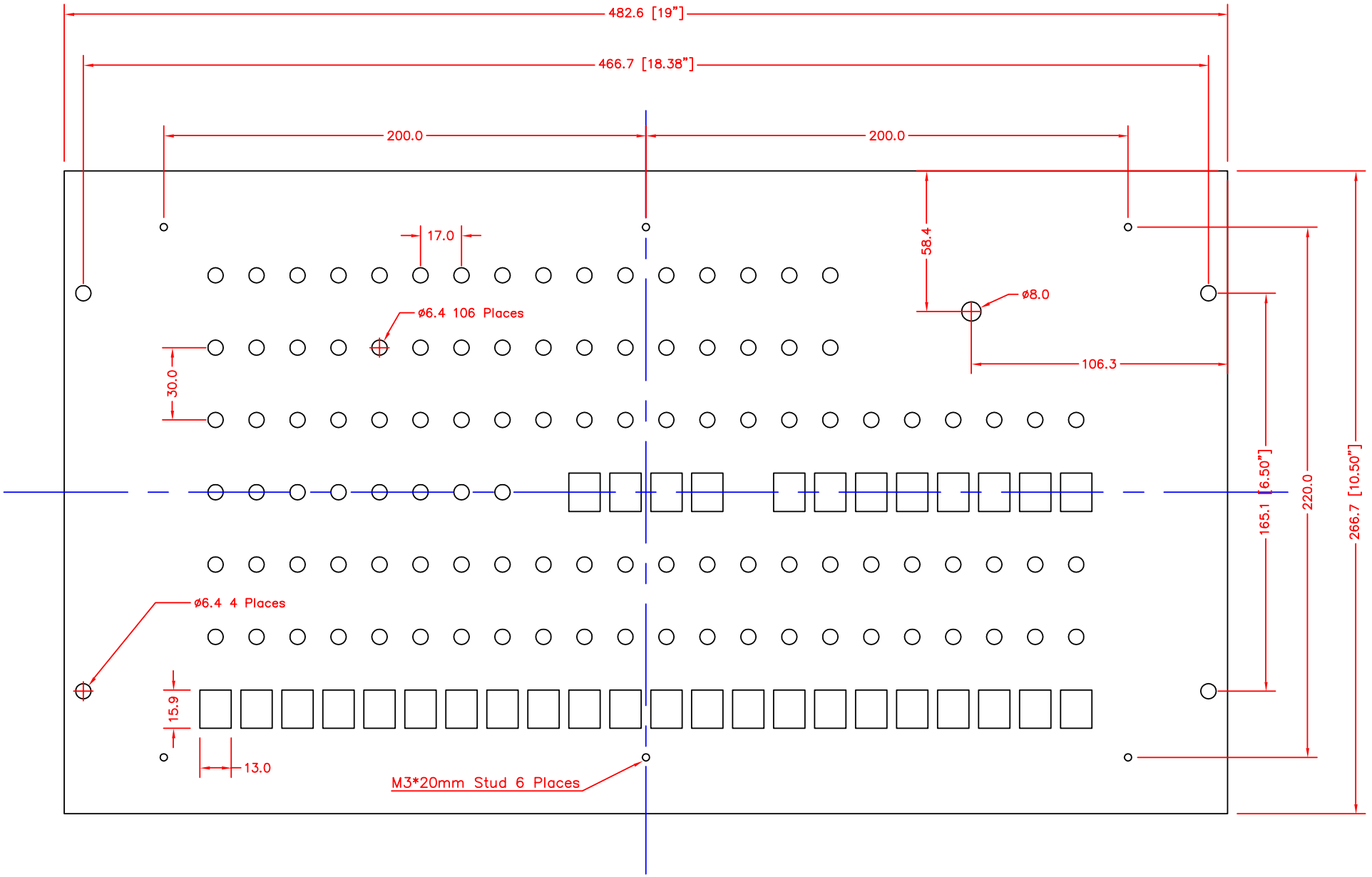
Ken Sumrall
Dave Conroy
Andrew Holme
Ben Franchuk
Gil Smith
Mark Atherton
Ron Watkins

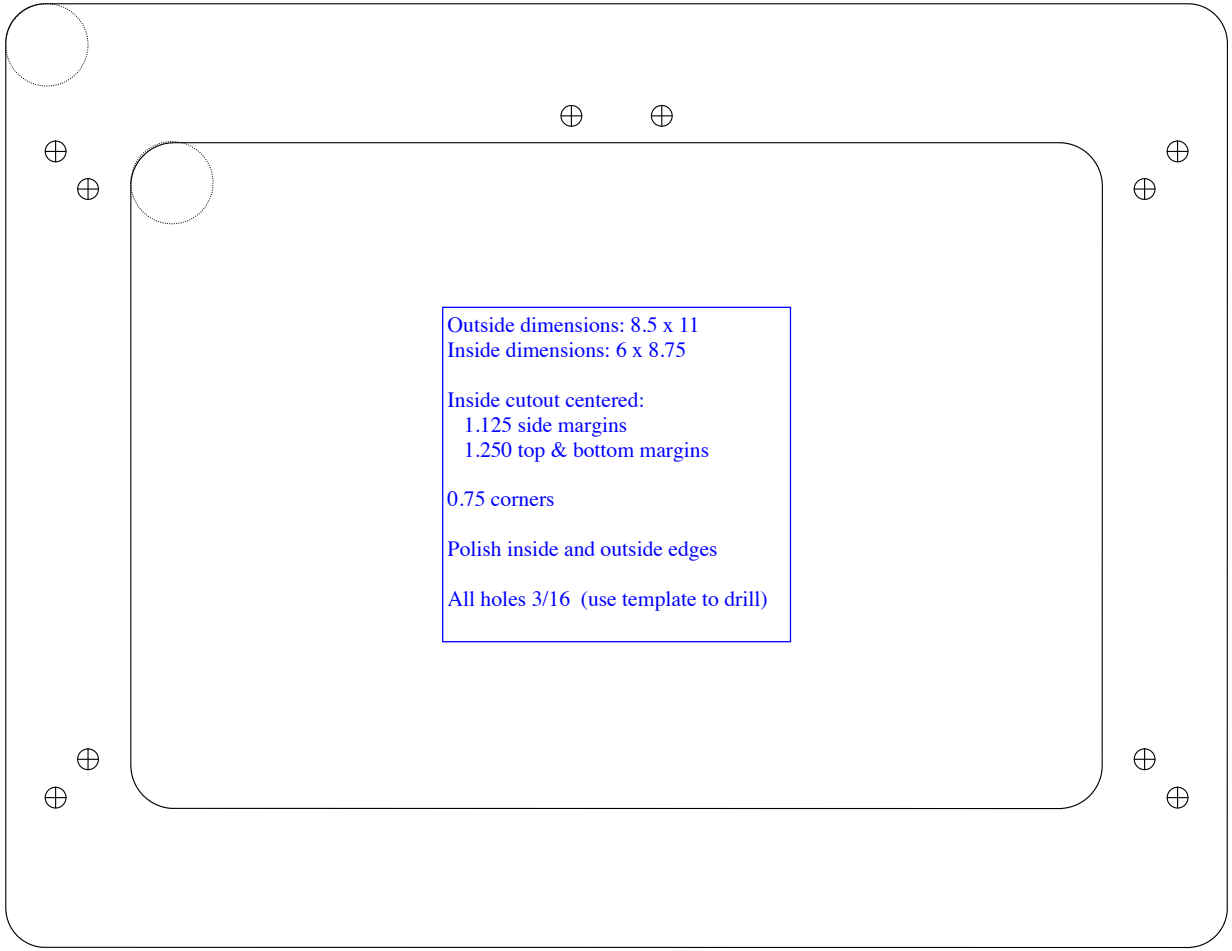
TTL Mark
Al Kossow
Simir Ribic
TriPheonix
Dave Brooks
Barry Cross
Ian White

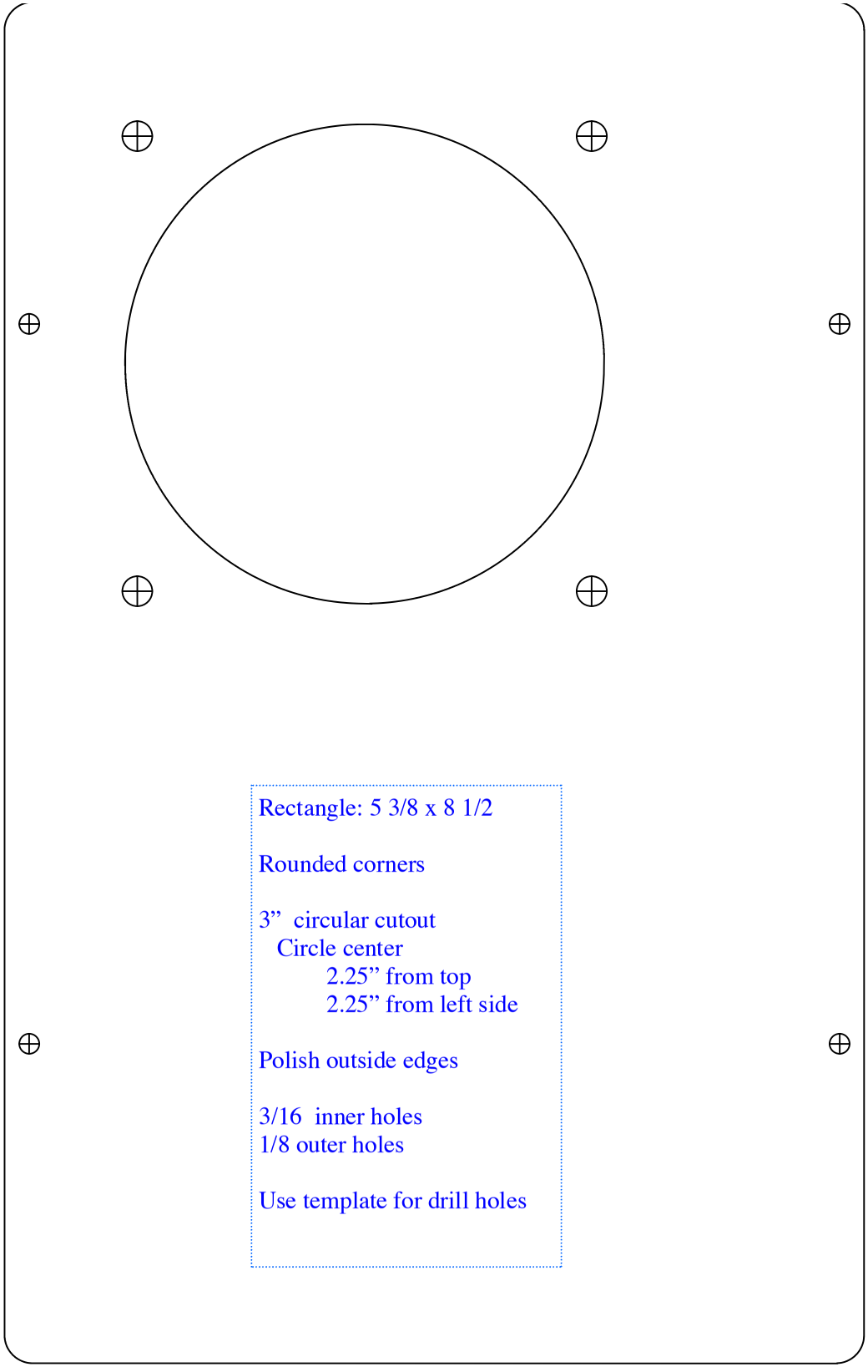
Attila Szabó
John Doran
Hans Summers
Dennis Kuschel
Merlin Skinner
...and many others
Thanks!



Clock Source	SW1	SW2
Alternate	Closed	Closed
3 Mhz	Open	Closed
Variable	Closed	Open
Single Step	Open	Open


482.6 [19"]
466.7 [18.38"]
200.0
200.0
17.0
58.4
ø8.0
ø6.4 106 Places
106.3
30.0
165.1 [6.50"]
220.0
266.7 [10.50"]
ø6.4 4 Places
15.9
13.0
M3*20mm Stud 6 Places


Outside dimensions: 8.5 x 11
Inside dimensions: 6 x 8.75
Inside cutout centered:
1.125 side margins
1.250 top & bottom margins
0.75 corners
Polish inside and outside edges
All holes 3/16 (use template to drill)



Rectangle: 5 3/8 x 8 1/2

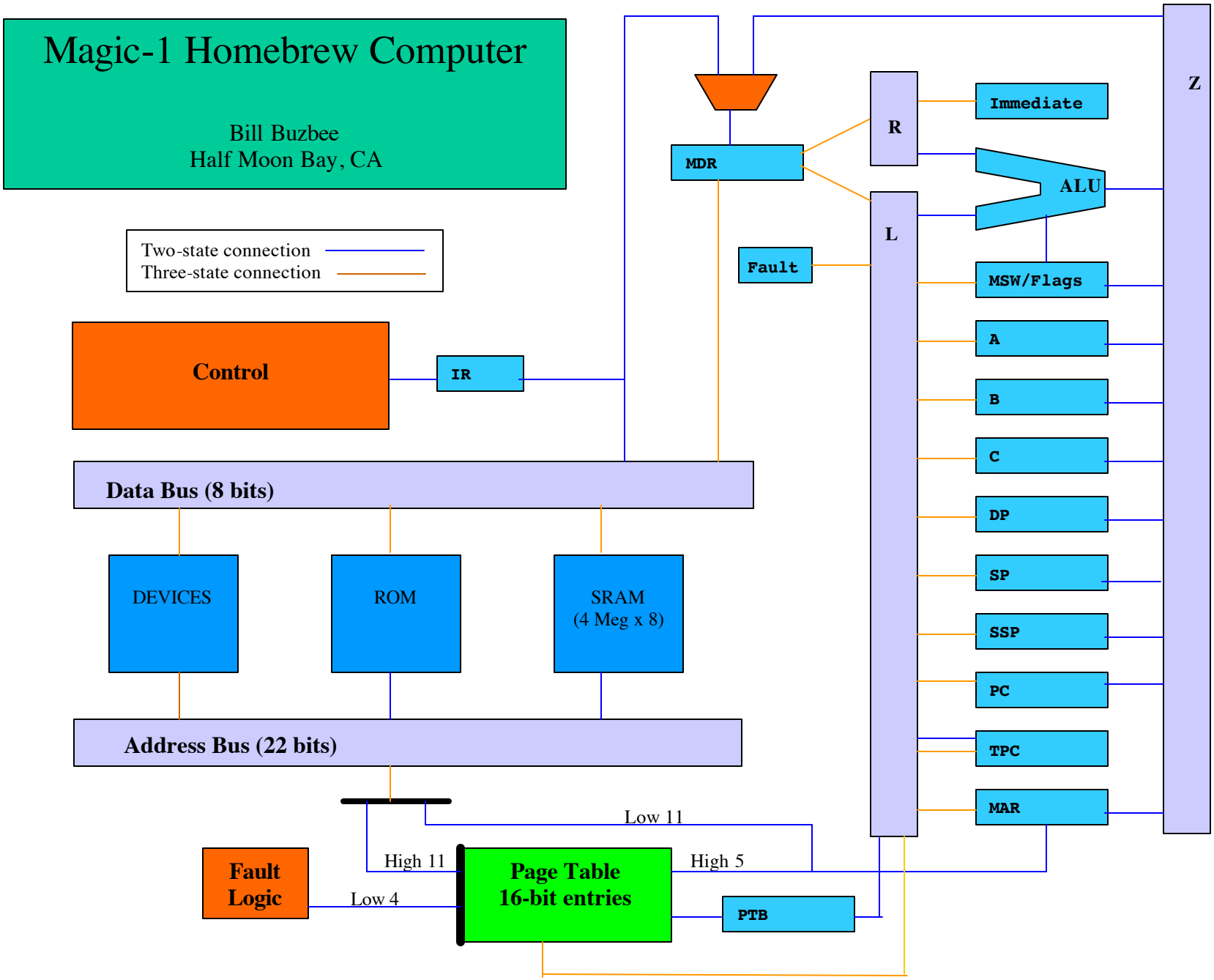
Rounded corners

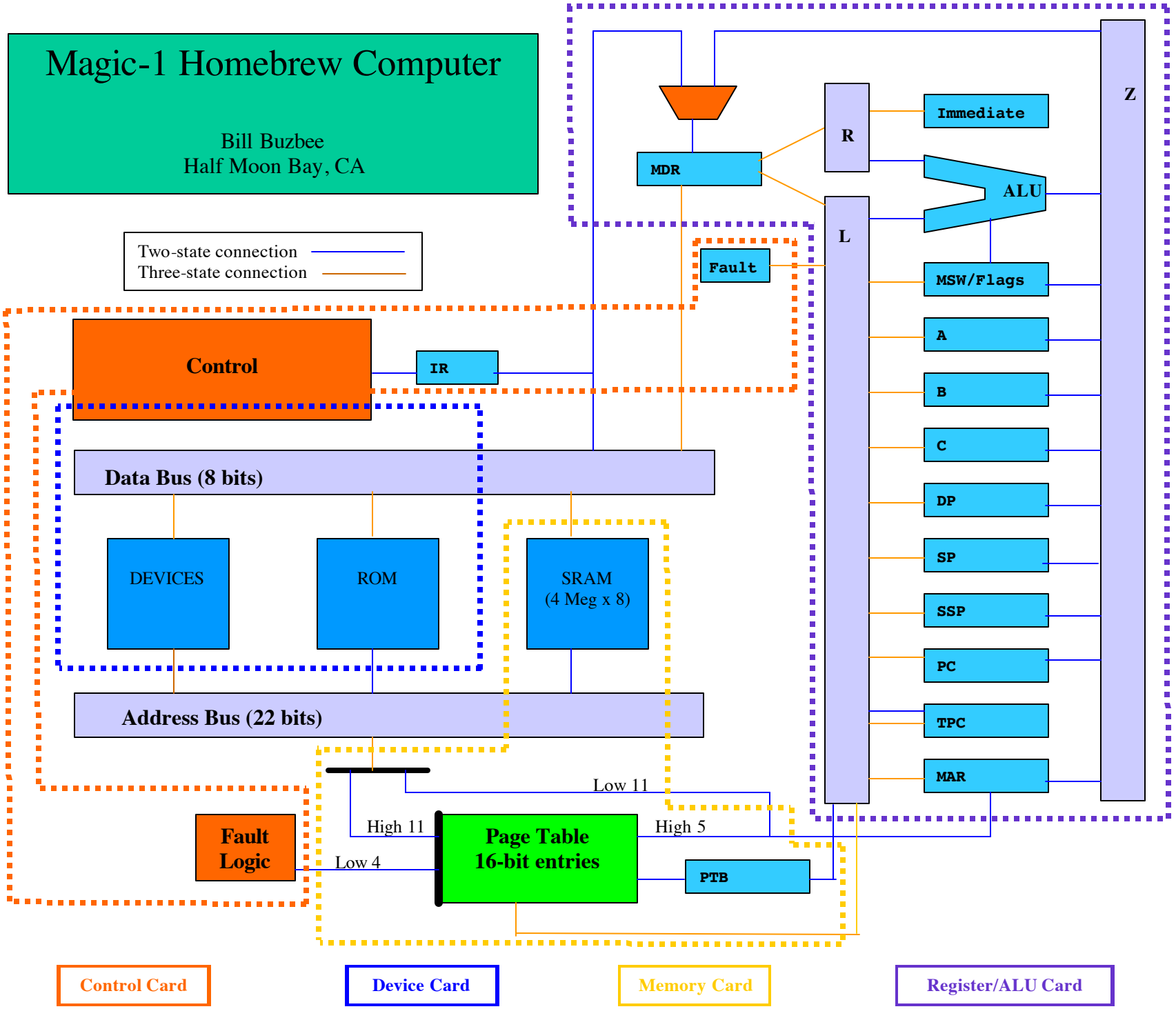
3” circular cutout
Circle center
2.25” from top
2.25” from left side

Polish outside edges

3/16 inner holes
1/8 outer holes

Use template for drill holes


Magic-1 Homebrew Computer
Bill Buzbee
Half Moon Bay, CA
Two-state connection
Three-state connection
Control
IR
MDR
R
Immediate
ALU
Z
L
Fault
MSW/Flags
A
B
C
DP
SP
SSP
PC
TPC
MAR
Data Bus (8 bits)
DEVICES
ROM
SRAM
(4 Meg x 8)
Address Bus (22 bits)
Low 11
High 11
High 5
Fault
Logic
Low 4
Page Table
16-bit entries
PTB


Magic-1 Homebrew Computer
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Half Moon Bay, CA
Two-state connection
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Control
IR
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MDR
R
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Low 11
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Low 4
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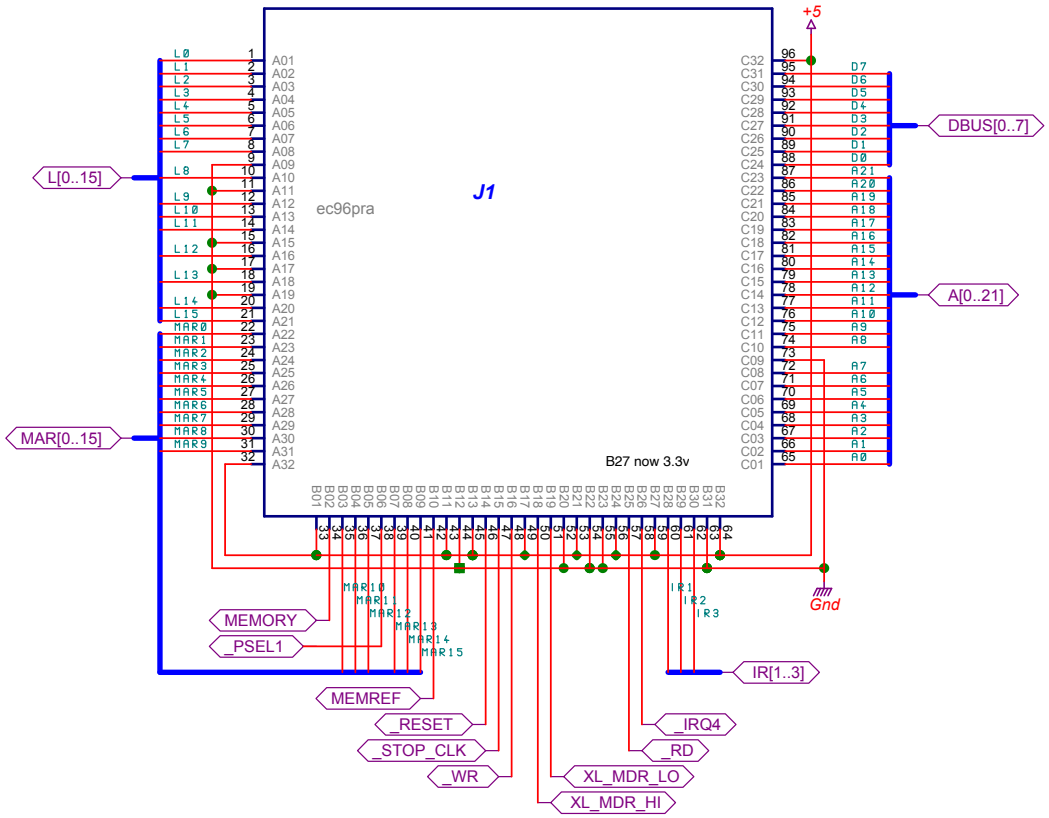
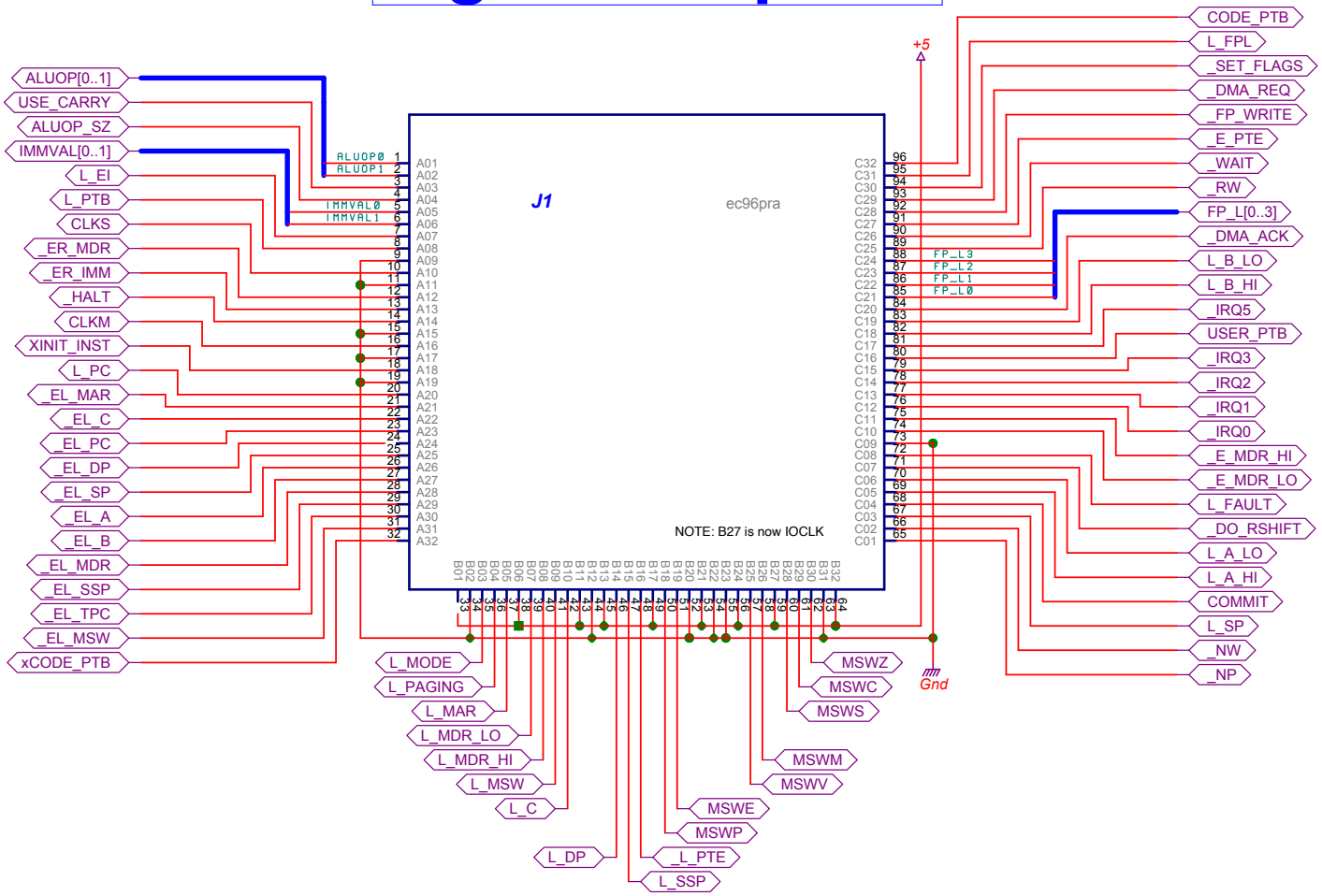
Page Table
16-bit entries
PTB
Control Card
Device Card
Memory Card
Register/ALU Card

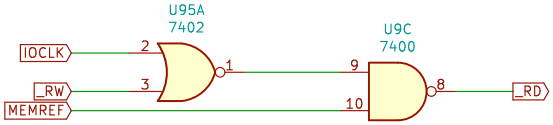
Left Backplane



Right Backplane

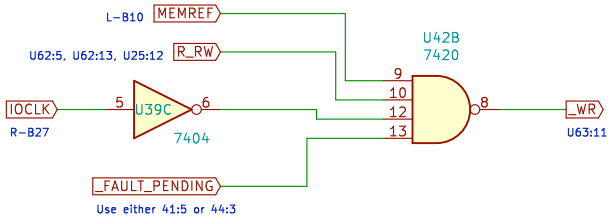


Front Panel Card modifications



_RD is generated on FP/Clock board. Pull 7432 from U95 position and replace with 7402. Use previously unused gate C from U9. Remove wires from pins 1, 2 & 3 of U95. Wire in new pins. To finish, run U9:8 to U5:4

Control Card modifications

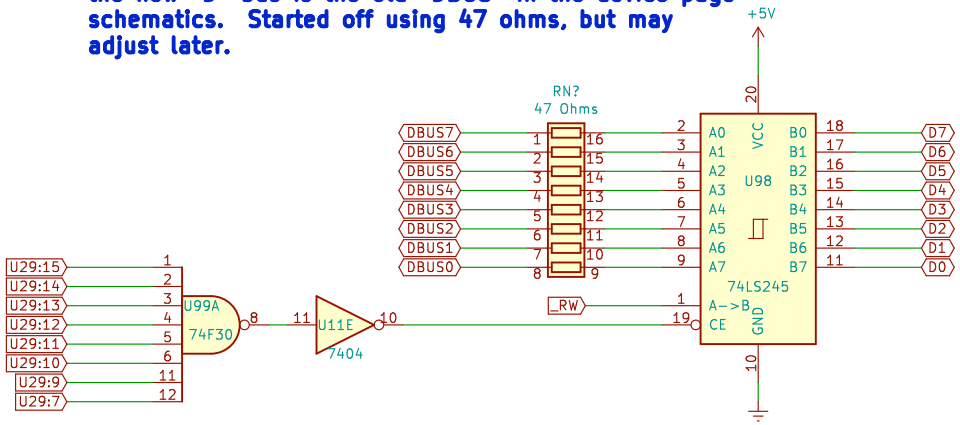


MEMREF previously used for PSEL computation and trap support. Perhaps factor it into _RD and _WR and don't use for PSEL? Main SRAM ties _OE to _RW, which is different than everyone else. Should it also use _RD? If so, do we run into timing issues? Device SRAM uses _RD, but can't handle fast clock with 70ns devices.

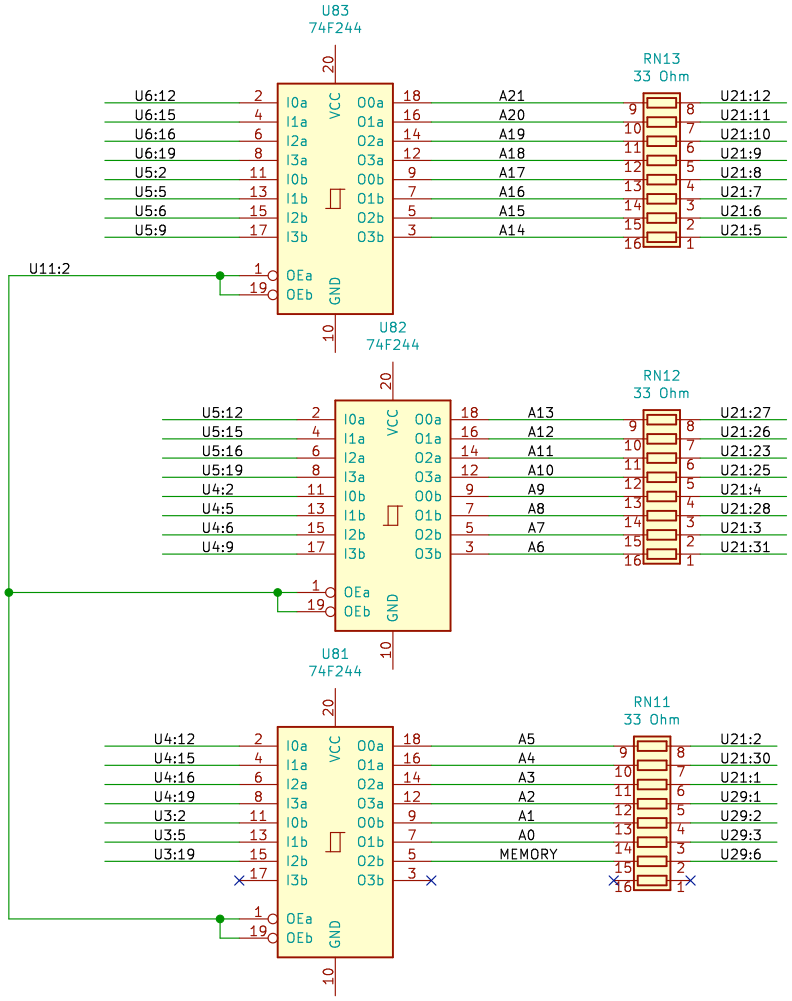
Sheet: / File: New_WR_RD.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6-0-10_14)		Id: 1/1

Memory Card Modifications

Added to memory card to provide partial termination for the data bus. Inserted between the existing DBUS net and the backplane edge connector. So, the new "D" bus is the old "DBUS" in the device page schematics. Started off using 47 ohms, but may adjust later.



Sheet: /		
File: Memory card rework.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6-0-10_14)		Id: 1/1



Memory card rework #2 – drivers & termination for address bus

Sheet: /		
File: Memory Card Rework 2.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6-0-10_14)		Id: 1/1

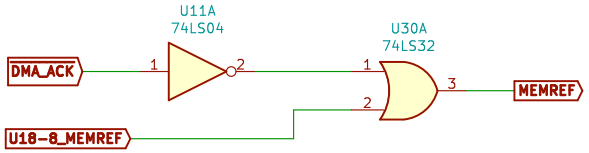
Memory Card Rework 3: MEMREF

Alter MEMREF to factor in DMA mode. This change restores the functionality of the front panel read/write following other changes that moved D and A bus signals behind buffers.

We pick up DMA_ACK from the existing inverted _DMA_ACK on U11–2. For the OR, we use an previously unused gate in U30.

MEMREF signal coming into the 7432 is the original one generated by U18–8 from the Page Table sheet, which is also disconnected from the backplane connector.

The new MEMREF signal is then connected to the backplane and used elsewhere in the system. Continue to use the old MEMREF in the generation of _WAIT, _NW and _NP internal to the memory card.

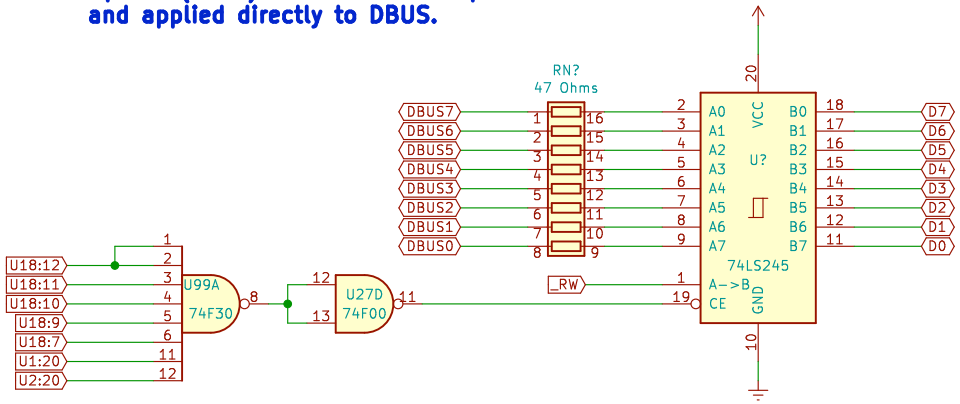


Sheet: /		
File: Memory Card Rework 3.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6–0–10_14)		Id: 1/1

Device Card Modifications

Added to device card to provide partial termination for the data bus. Inserted between the existing DBUS net and the backplane edge connector. So, the new "D" bus is the old "DBUS" in the device page schematics. Started off using 47 ohms, but may adjust later.

Update (2023). Removed front panel switches from 74F30 and applied directly to DBUS.



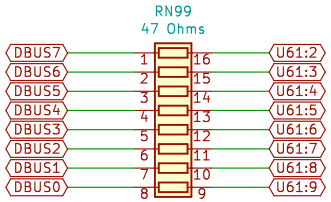
Sheet: /
File: Device card rework.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6-0-10_14)		Id: 1/1

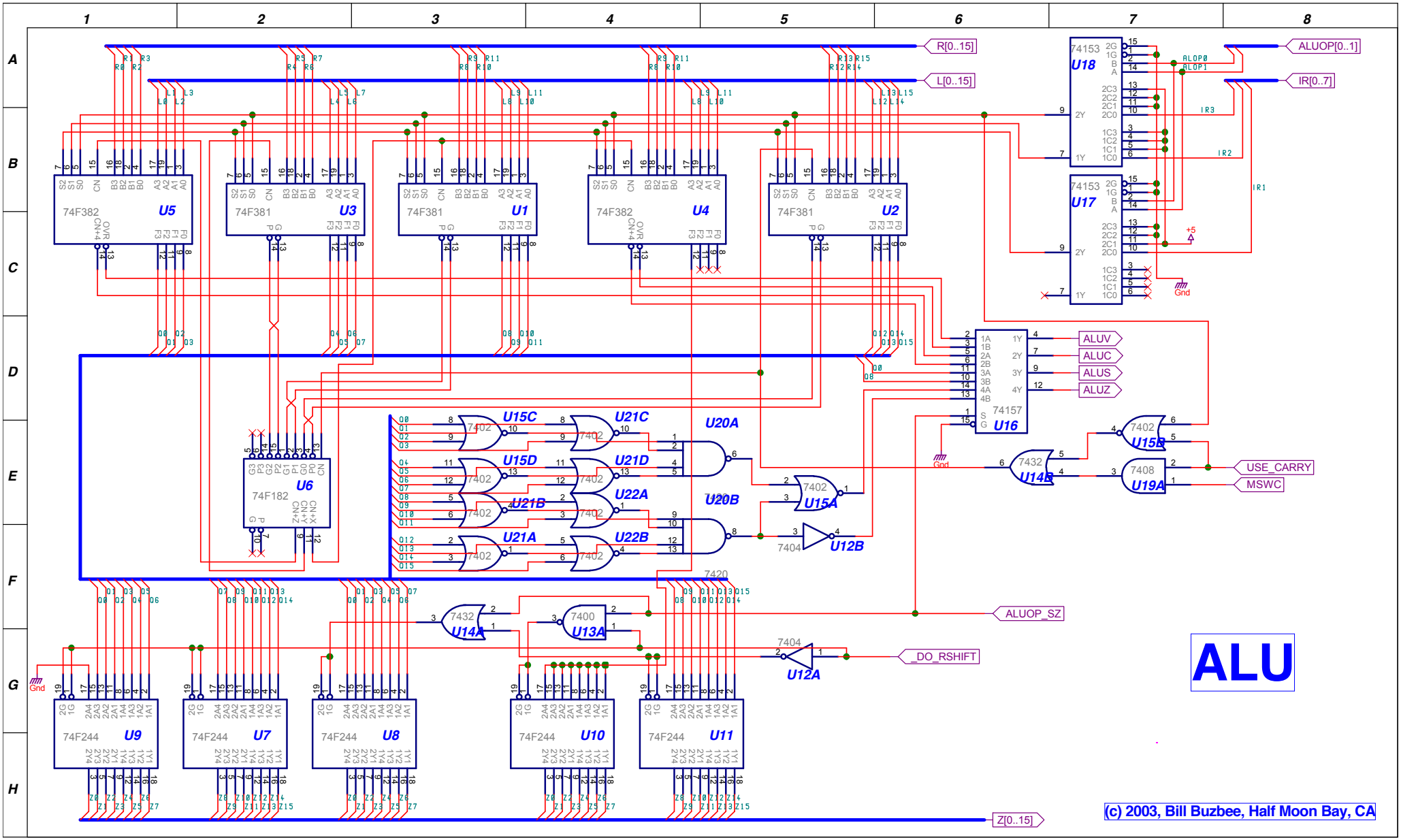
Register Card Modifications

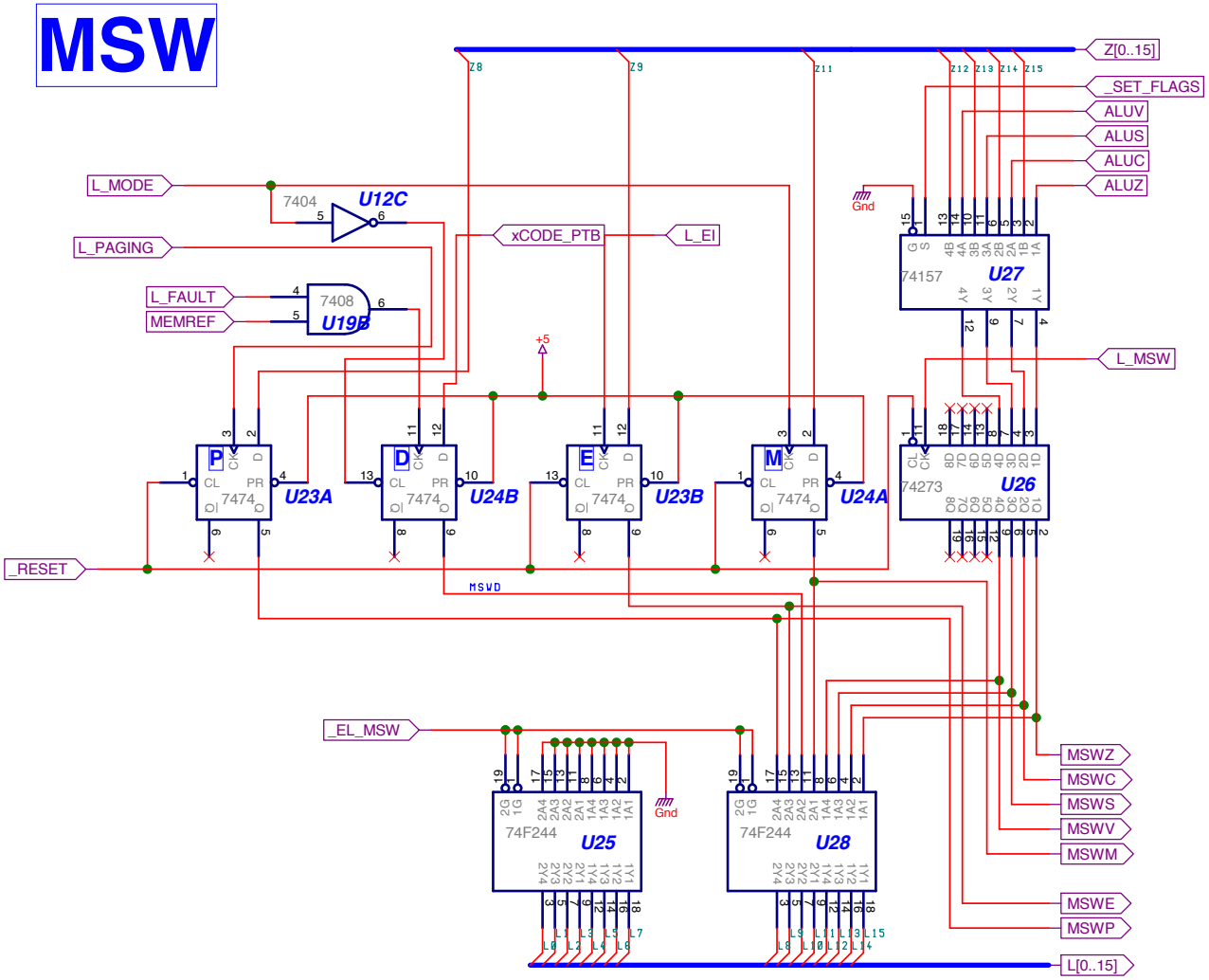
Added series termination to existing 74245 bi-direcitonal bus driver. Start with 47 Ohms, but may adjust later.

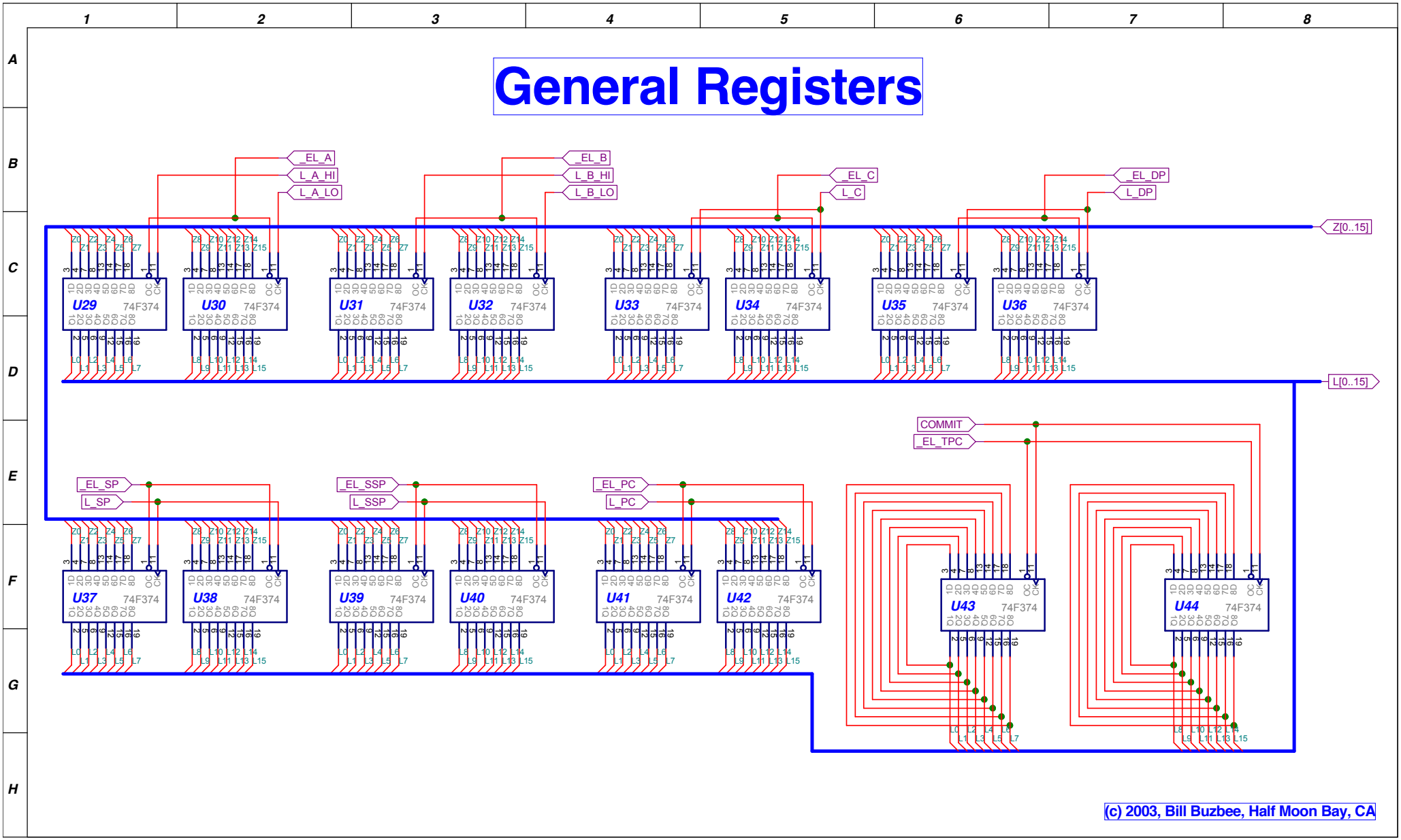


Sheet: /		
File: Register card rework.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6-0-10_14)		Id: 1/1

Register/ALU Card


ALU
R[0..15]
L[0..15]
ALUOP[0..1]
IR[0..7]
ALUOP_SZ
_DO_RSHIFT
Z[0..15]
USE_CARRY
MSWC
ALUV
ALUC
ALUS
ALUZ
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12A
U12B
U13A
U14A
U14B
U15A
U15B
U15C
U15D
U16
U17
U18
U19A
U20A
U20B
U21A
U21B
U21C
U21D
U22A
U22B
74F382
74F381
74F182
74F244
74157
74153
7402
7404
7408
7420
7432
7400
Gnd
+5
(c) 2003, Bill Buzbee, Half Moon Bay, CA




General Registers
_EL_A
L_A_HI
L_A_LO
_EL_B
L_B_HI
L_B_LO
_EL_C
L_C
_EL_DP
L_DP
Z[0..15]
L[0..15]
COMMIT
_EL_TPC
_EL_SP
L_SP
_EL_SSP
L_SSP
_EL_PC
L_PC
U29 74F374
U30 74F374
U31 74F374
U32 74F374
U33 74F374
U34 74F374
U35 74F374
U36 74F374
U37 74F374
U38 74F374
U39 74F374
U40 74F374
U41 74F374
U42 74F374
U43 74F374
U44 74F374
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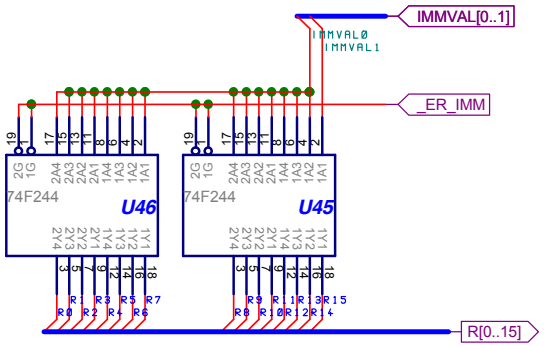
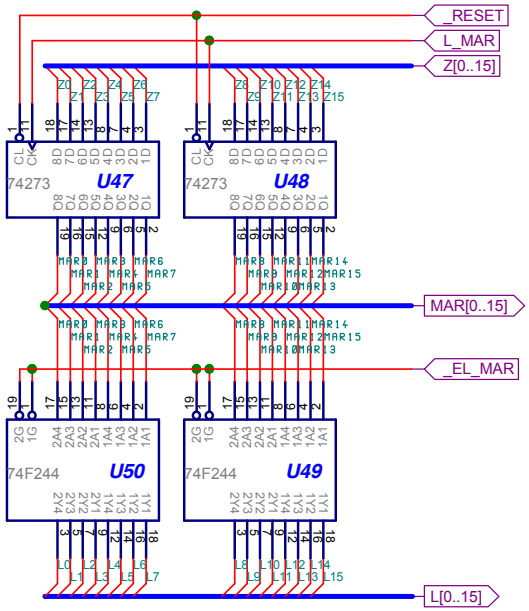
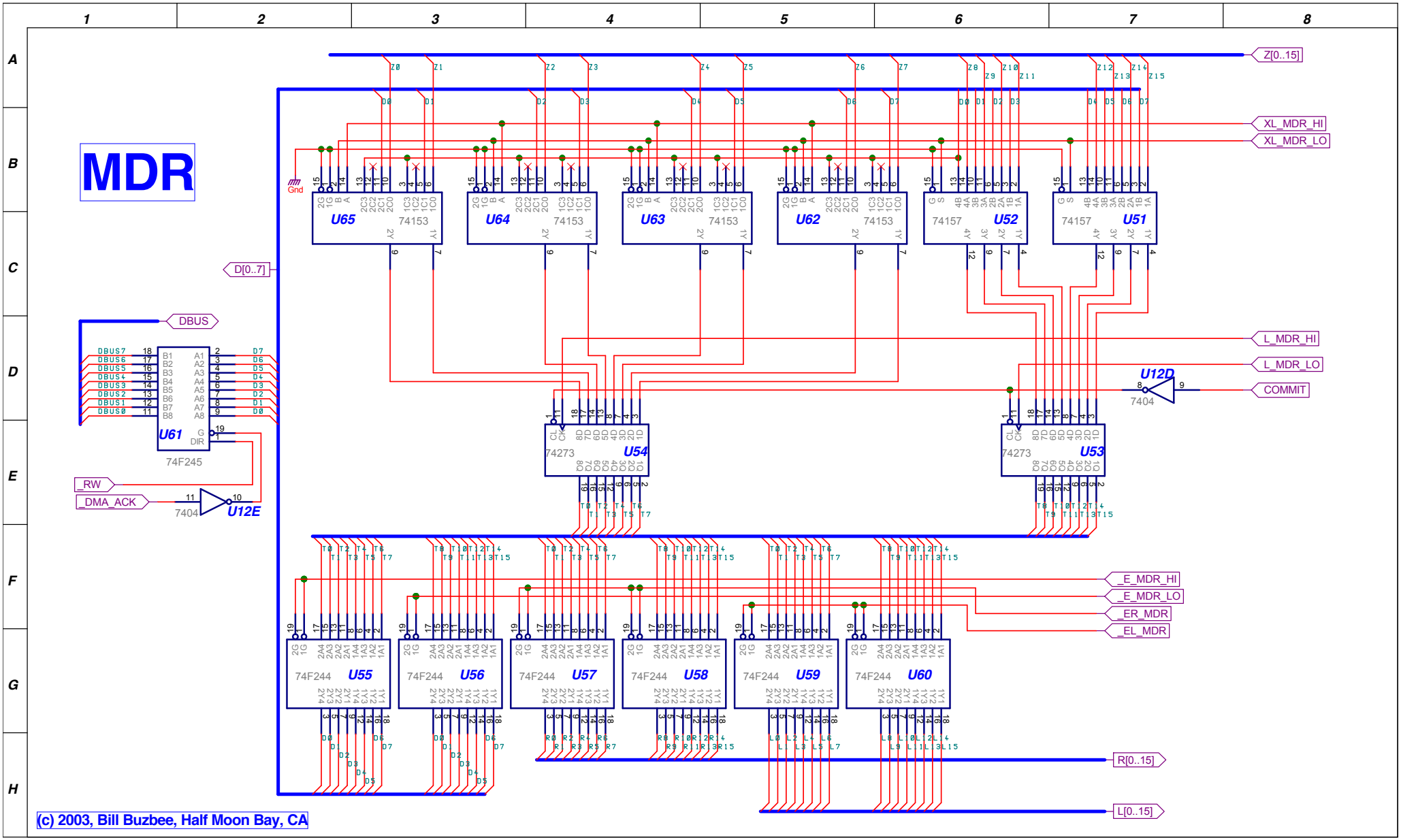
Special Registers






MDR
Z[0..15]
XL_MDR_HI
XL_MDR_LO
D[0..7]
DBUS
L_MDR_HI
L_MDR_LO
COMMIT
_RW
_DMA_ACK
_E_MDR_HI
_E_MDR_LO
_ER_MDR
_EL_MDR
R[0..15]
L[0..15]
Gnd
U65
U64
U63
U62
U52
U51
U61
U12D
U12E
U54
U53
U55
U56
U57
U58
U59
U60
74153
74157
74245
74273
74244
7404
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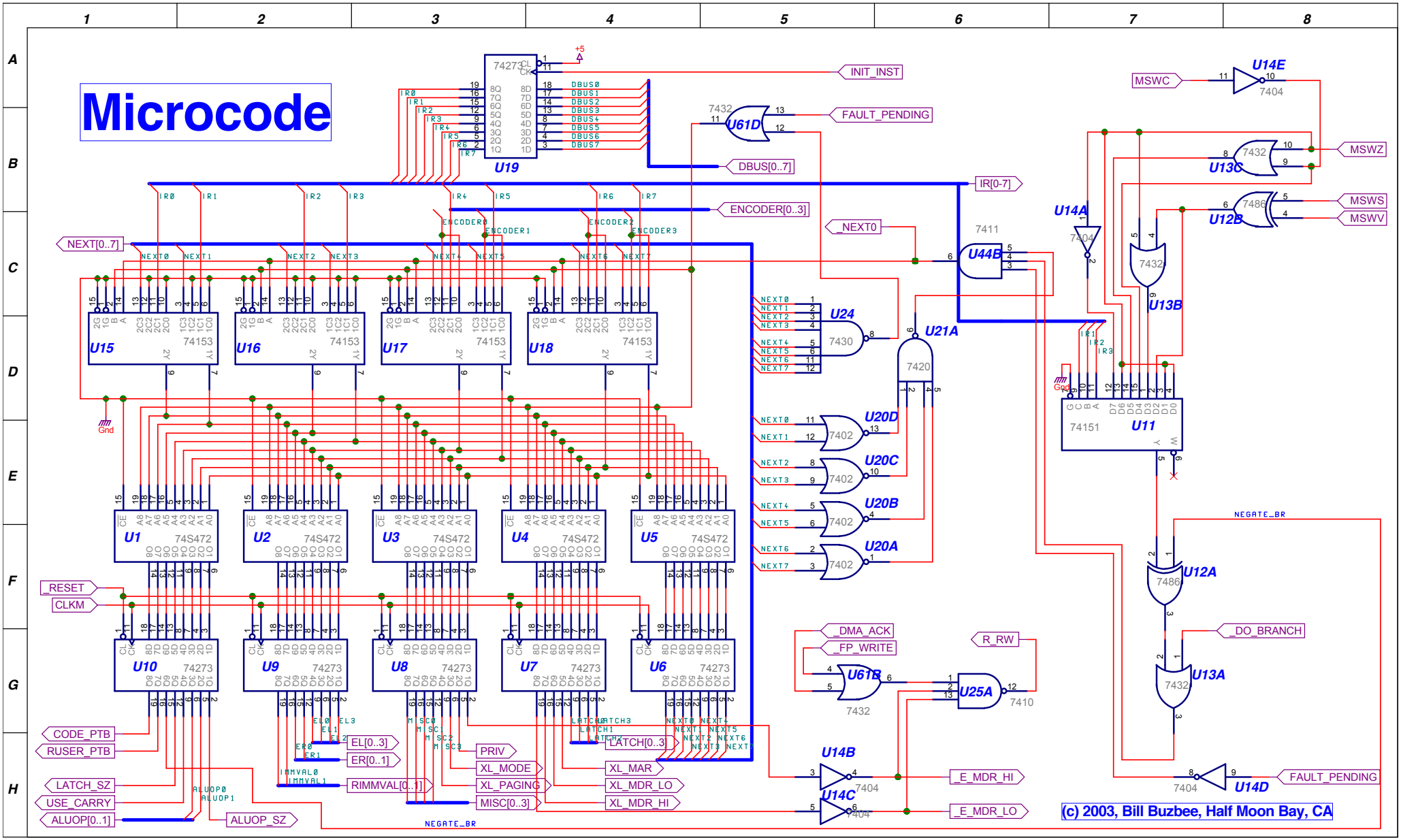
Register card BOM

Item	Qty	References	Value
1	1	U13	7400
2	3	U15,U21,U22	7402
3	1	U12	7404
4	1	U19	7408
5	1	U20	7420
6	1	U14	7432
7	2	U23,U24	7474
8	6	U17,U18,U62,U63,U64,U65	74153
9	4	U16,U27,U51,U52	74157
10	5	U26,U47,U48,U53,U54	74273
11	1	U6	74F182
12	17	U7,U8,U9,U10,U11,U25,U28,U45,U46,U49,U50,U55,U56, U57,U58,U59,U60	74F244
13	1	U61	74F245
14	16	U29,U30,U31,U32,U33,U34,U35,U36,U37,U38,U39,U40,U41, U42,U43,U44	74F374
15	3	U1,U2,U3	74F381
16	2	U4,U5	74F382

Control Card


Microcode
U19
U61D
U15
U16
U17
U18
U1
U2
U3
U4
U5
U10
U9
U8
U7
U6
U24
U21A
U20D
U20C
U20B
U20A
U44B
U14A
U14E
U13C
U12B
U13B
U11
U12A
U13A
U61B
U25A
U14B
U14C
U14D
INIT_INST
FAULT_PENDING
DBUS[0..7]
IR[0-7]
ENCODER[0..3]
NEXT[0..7]
_NEXT0
MSWC
MSWZ
MSWS
MSWV
_RESET
CLKM
_DMA_ACK
_FP_WRITE
R_RW
_DO_BRANCH
NEGATE_BR
CODE_PTB
RUSER_PTB
LATCH_SZ
USE_CARRY
ALUOP[0..1]
ALUOP_SZ
EL[0..3]
ER[0..1]
RIMMVAL[0..1]
PRIV
XL_MODE
XL_PAGING
MISC[0..3]
LATCH[0..3]
XL_MAR
XL_MDR_LO
XL_MDR_HI
_E_MDR_HI
_E_MDR_LO
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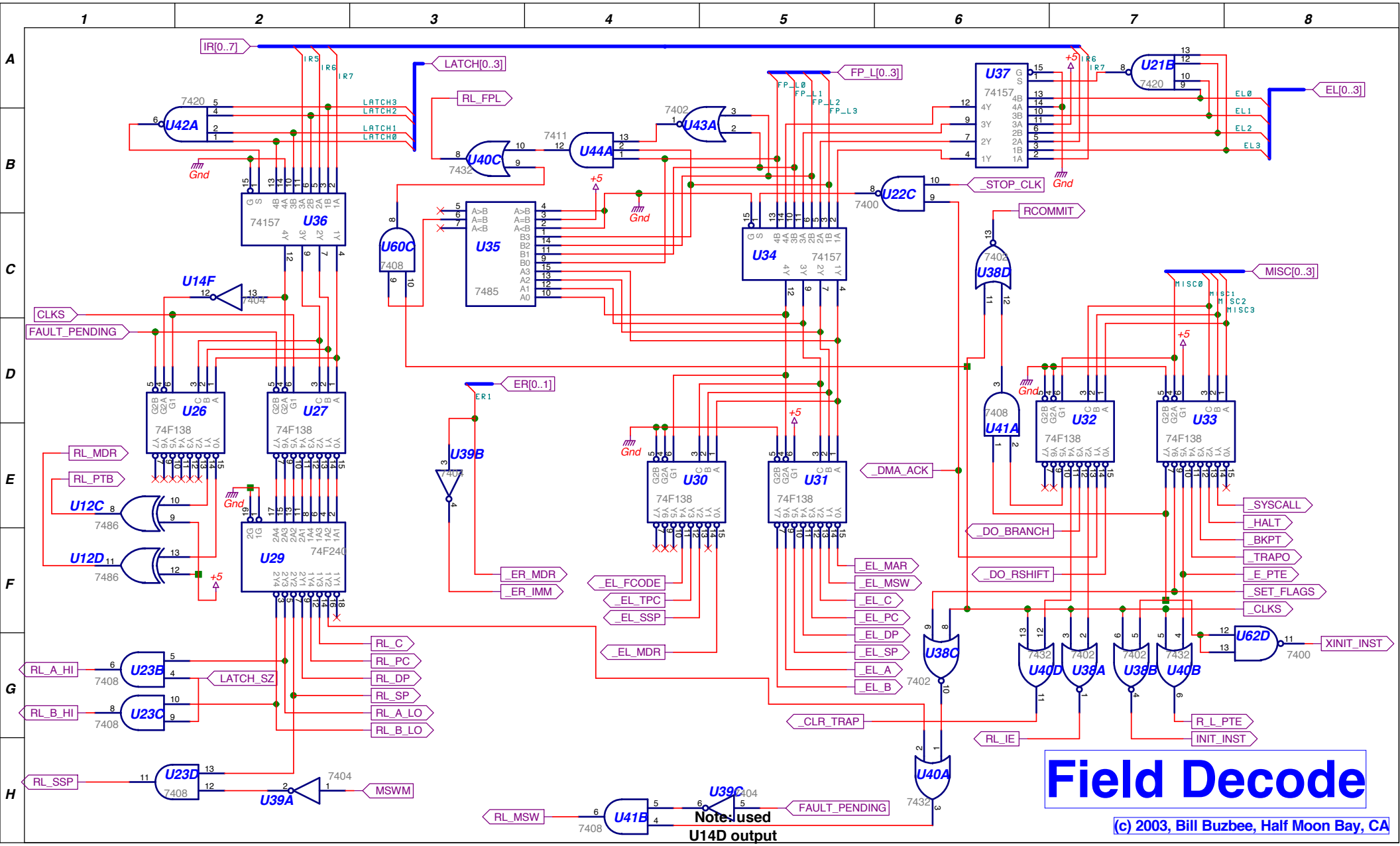
IR[0..7]
LATCH[0..3]
RL_FPL
FP_L[0..3]
EL[0..3]
MISC[0..3]
U42A
U40C
U44A
U43A
U37
U21B
U36
U35
U34
U22C
_STOP_CLK
RCOMMIT
U60C
U38D
U14F
CLKS
FAULT_PENDING
U26
U27
U39B
ER[0..1]
_ER_MDR
_ER_IMM
U30
U31
U41A
U32
U33
_DMA_ACK
_DO_BRANCH
_DO_RSHIFT
_SYSCALL
_HALT
_BKPT
_TRAPO
_E_PTE
_SET_FLAGS
_CLKS
RL_MDR
RL_PTB
U12C
U12D
U29
_EL_FCODE
_EL_TPC
_EL_SSP
_EL_MDR
_EL_MAR
_EL_MSW
_EL_C
_EL_PC
_EL_DP
_EL_SP
_EL_A
_EL_B
U38C
U40D
U38A
U38B
U40B
U62D
XINIT_INST
R_L_PTE
INIT_INST
RL_IE
_CLR_TRAP
U40A
RL_A_HI
RL_B_HI
U23B
U23C
LATCH_SZ
RL_C
RL_PC
RL_DP
RL_SP
RL_A_LO
RL_B_LO
RL_SSP
U23D
U39A
MSWM
RL_MSW
U41B
U39C
FAULT_PENDING
Note: Used U14D output
Field Decode
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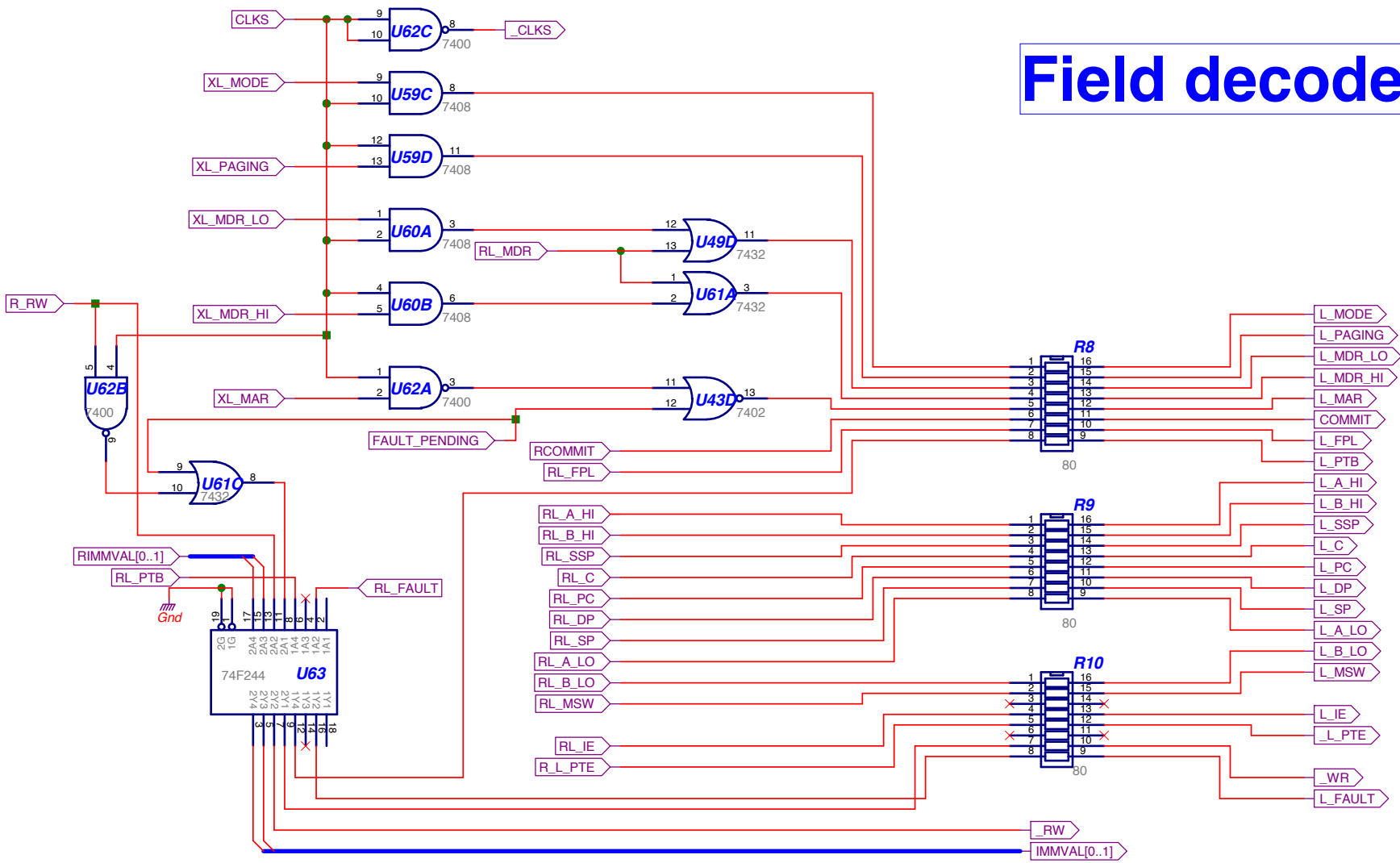
Field decode 2
CLKS
U62C
7400
_CLKS
XL_MODE
U59C
7408
XL_PAGING
U59D
7408
XL_MDR_LO
U60A
7408
RL_MDR
U49D
7432
U61A
7432
R_RW
XL_MDR_HI
U60B
7408
U62B
7400
XL_MAR
U62A
7400
U43D
7402
FAULT_PENDING
RCOMMIT
RL_FPL
U61C
7432
RIMMVAL[0..1]
RL_PTB
Gnd
RL_FAULT
74F244
U63
RL_A_HI
RL_B_HI
RL_SSP
RL_C
RL_PC
RL_DP
RL_SP
RL_A_LO
RL_B_LO
RL_MSW
RL_IE
R_L_PTE
R8
R9
R10
80
L_MODE
L_PAGING
L_MDR_LO
L_MDR_HI
L_MAR
COMMIT
L_FPL
L_PTB
L_A_HI
L_B_HI
L_SSP
L_C
L_PC
L_DP
L_SP
L_A_LO
L_B_LO
L_MSW
L_IE
_L_PTE
_WR
L_FAULT
_RW
IMMVAL[0..1]
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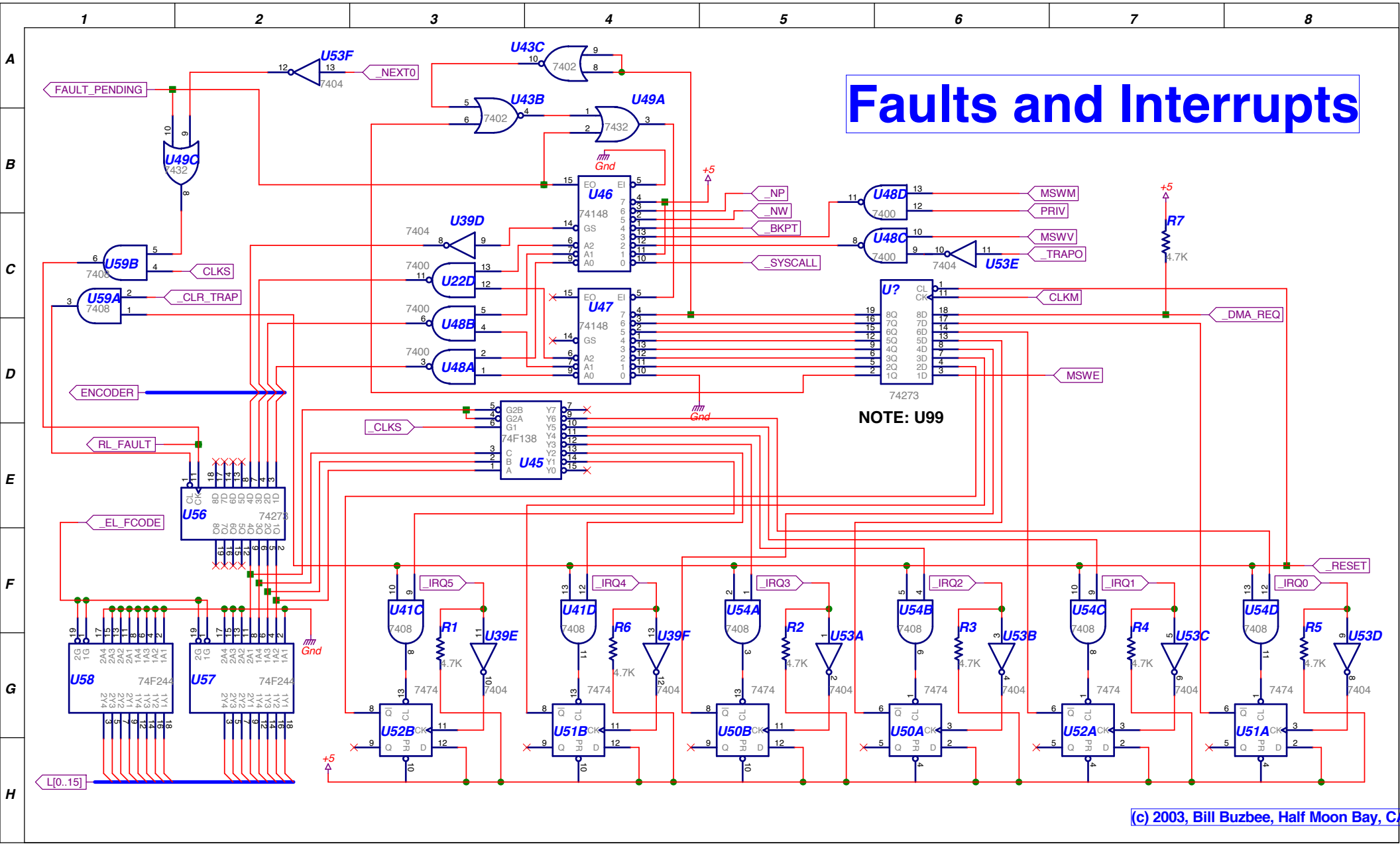
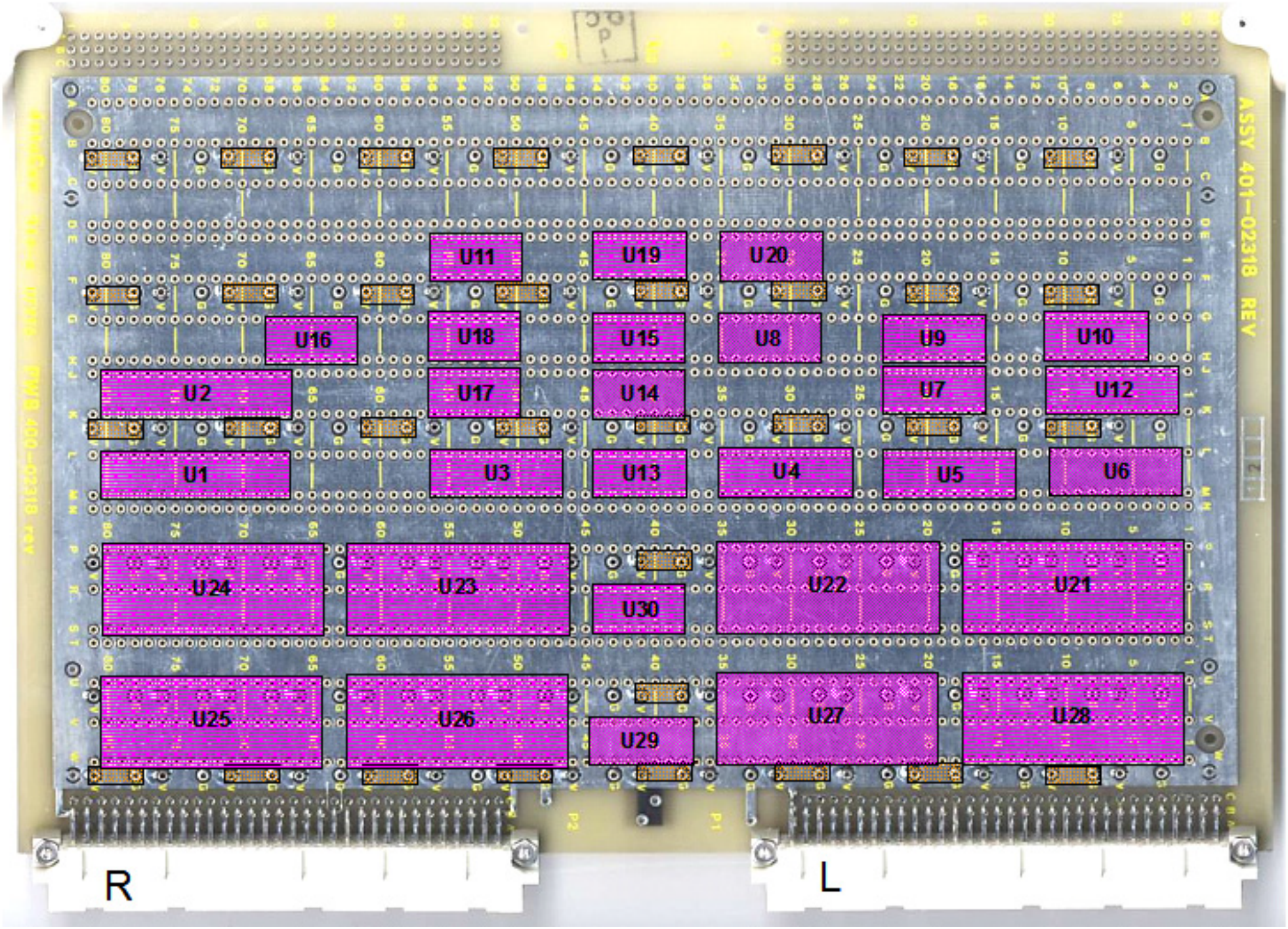

Faults and Interrupts
FAULT_PENDING
_NEXT0
U53F
7404
U43C
7402
U43B
7402
U49A
7432
U49C
7432
Gnd
+5
U46
74148
U47
74148
_NP
_NW
_BKPT
_SYSCALL
U39D
7404
U22D
7400
U48B
7400
U48A
7400
U59B
7408
CLKS
U59A
7408
_CLR_TRAP
U48D
7400
U48C
7400
U53E
7404
MSWM
PRIV
MSWV
_TRAPO
R7
4.7K
U?
74273
CLKM
_DMA_REQ
MSWE
NOTE: U99
ENCODER
RL_FAULT
_CLKS
U45
74F138
U56
74273
_EL_FCODE
U58
74F244
U57
74F244
L[0..15]
_IRQ5
_IRQ4
_IRQ3
_IRQ2
_IRQ1
_IRQ0
_RESET
U41C
U41D
U54A
U54B
U54C
U54D
R1
R6
R2
R3
R4
R5
U39E
U39F
U53A
U53B
U53C
U53D
7474
U52B
U51B
U50B
U50A
U52A
U51A
(c) 2003, Bill Buzbee, Half Moon Bay, C

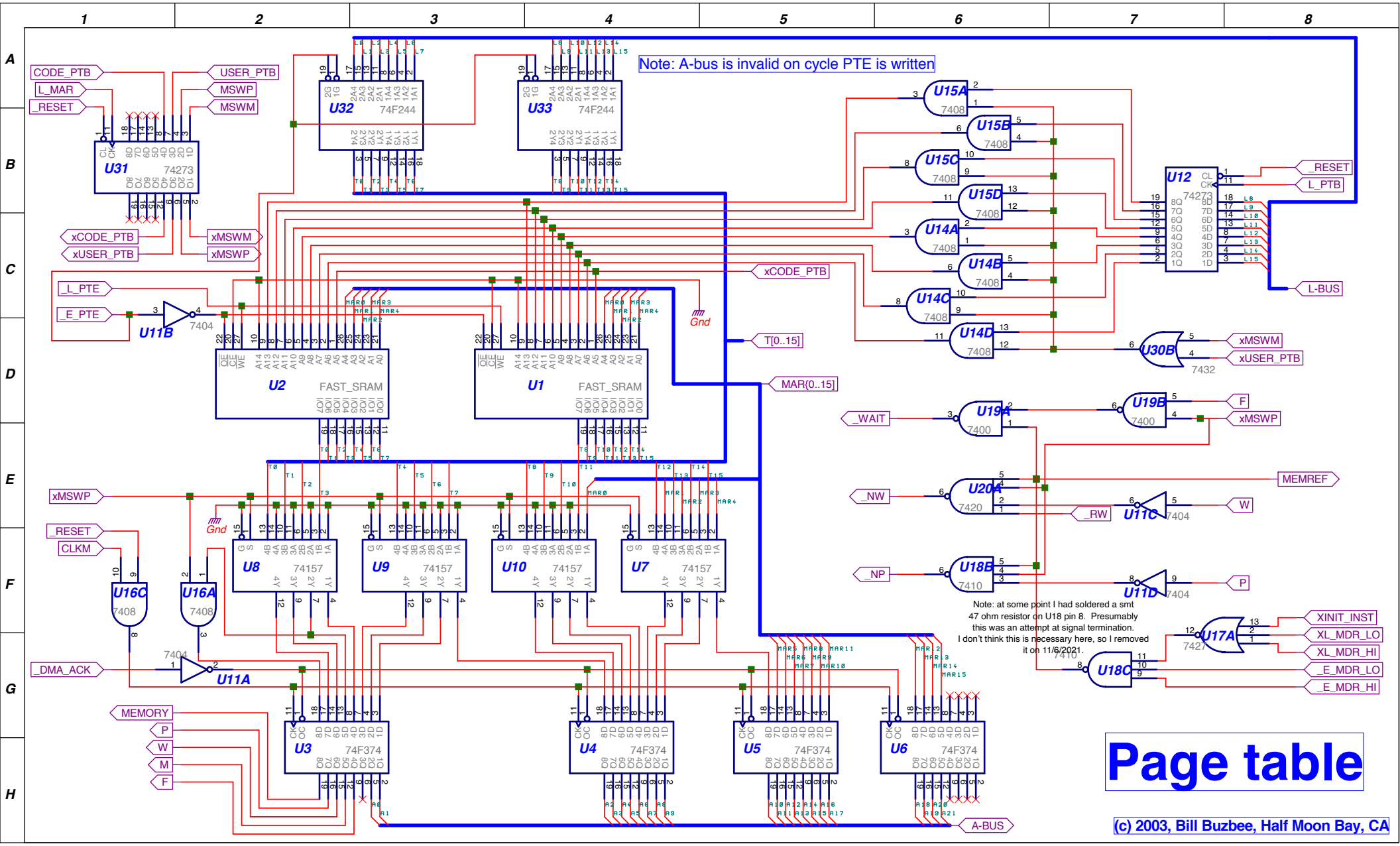
Control card BOM

Item	Qty	References	Value
1	3	R8,R9,R10	80
2	7	R1,R2,R3,R4,R5,R6,R7	4.7K
3	3	U22,U48,U62	7400
4	3	U20,U38,U43	7402
5	3	U14,U39,U53	7404
6	5	U23,U41,U54,U59,U60	7408
7	1	U25	7410
8	1	U44	7411
9	2	U21,U42	7420
10	1	U24	7430
11	4	U13,U40,U49,U61	7432
12	4	U50,U51,U52,U55	7474
13	1	U35	7485
14	1	U12	7486
15	2	U46,U47	74148
16	1	U11	74151
17	4	U15,U16,U17,U18	74153
18	3	U34,U36,U37	74157
19	7	U6,U7,U8,U9,U10,U19,U56	74273
20	7	U26,U27,U30,U31,U32,U33,U45	74F138
21	1	U29	74F240
22	3	U57,U58,U63	74F244
23	5	U1,U2,U3,U4,U5	74S472

Note: U64 and U28 deleted

Memory Card


U11
U19
U20
U16
U18
U15
U8
U9
U10
U2
U17
U14
U7
U12
U1
U3
U13
U4
U5
U6
U24
U23
U22
U21
U30
U25
U26
U27
U28
U29
R
L
ASSY 401-02318 REV


Note: A-bus is invalid on cycle PTE is written
CODE_PTB
L_MAR
_RESET
USER_PTB
MSWP
MSWM
U31 74273
U32 74F244
U33 74F244
xCODE_PTB
xUSER_PTB
xMSWM
xMSWP
_L_PTE
_E_PTE
U11B 7404
U2 FAST_SRAM
U1 FAST_SRAM
Gnd
T[0..15]
MAR{0..15]
U15A 7408
U15B 7408
U15C 7408
U15D 7408
U14A 7408
U14B 7408
U14C 7408
U14D 7408
U12 74273
_RESET
L_PTB
L-BUS
U30B 7432
xMSWM
xUSER_PTB
_WAIT
U19A 7400
U19B 7400
F
xMSWP
MEMREF
_NW
U20A 7420
_RW
U11C 7404
W
_NP
U18B 7410
U11D 7404
P
Note: at some point I had soldered a smt
47 ohm resistor on U18 pin 8. Presumably
this was an attempt at signal termination.
I don't think this is necessary here, so I removed
it on 11/6/2021.
U17A 7427
U18C 7410
XINIT_INST
XL_MDR_LO
XL_MDR_HI
_E_MDR_LO
_E_MDR_HI
_RESET
CLKM
U16C 7408
U16A 7408
U11A 7404
_DMA_ACK
U8 74157
U9 74157
U10 74157
U7 74157
MEMORY
P
W
M
F
U3 74F374
U4 74F374
U5 74F374
U6 74F374
A-BUS
Page table
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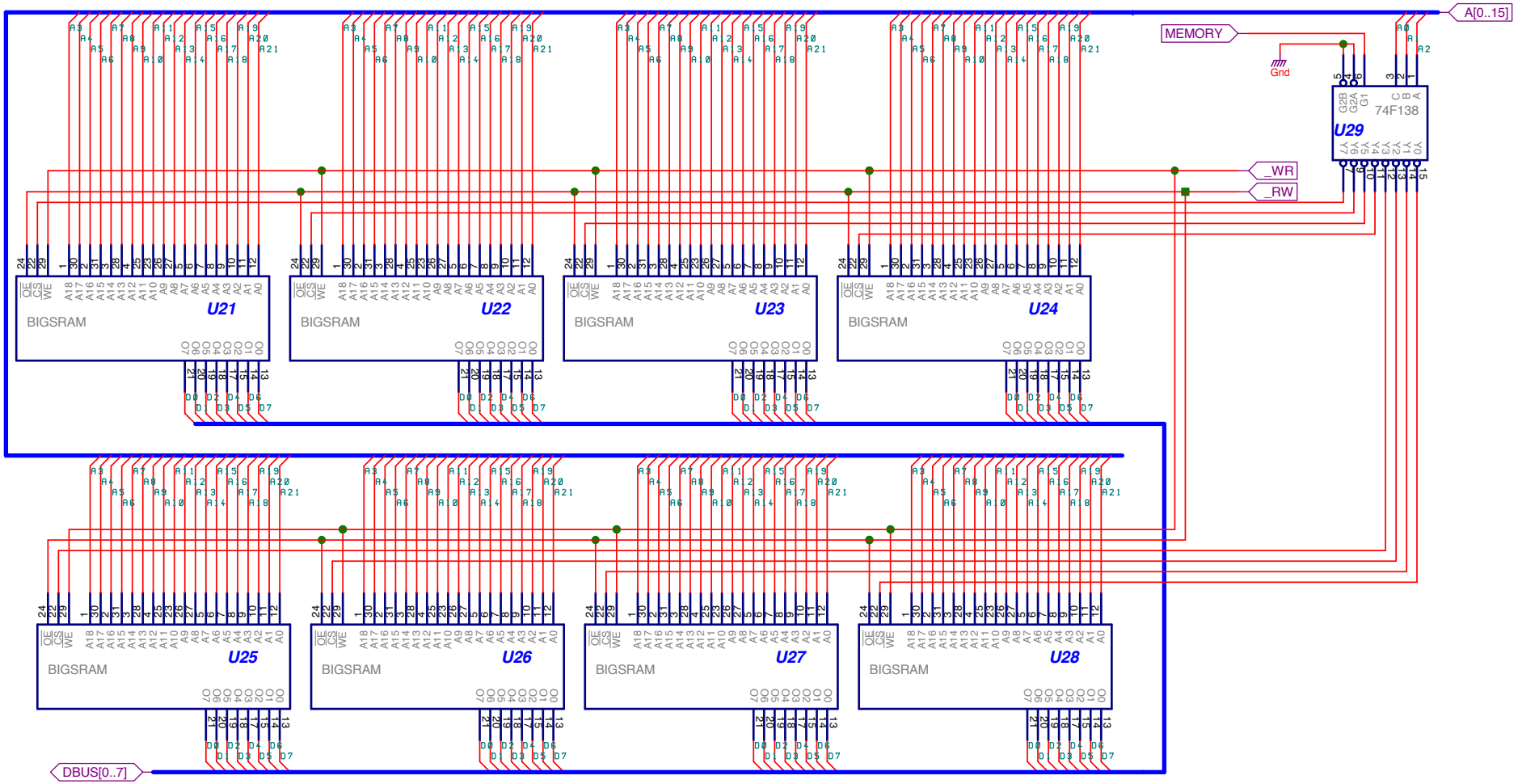
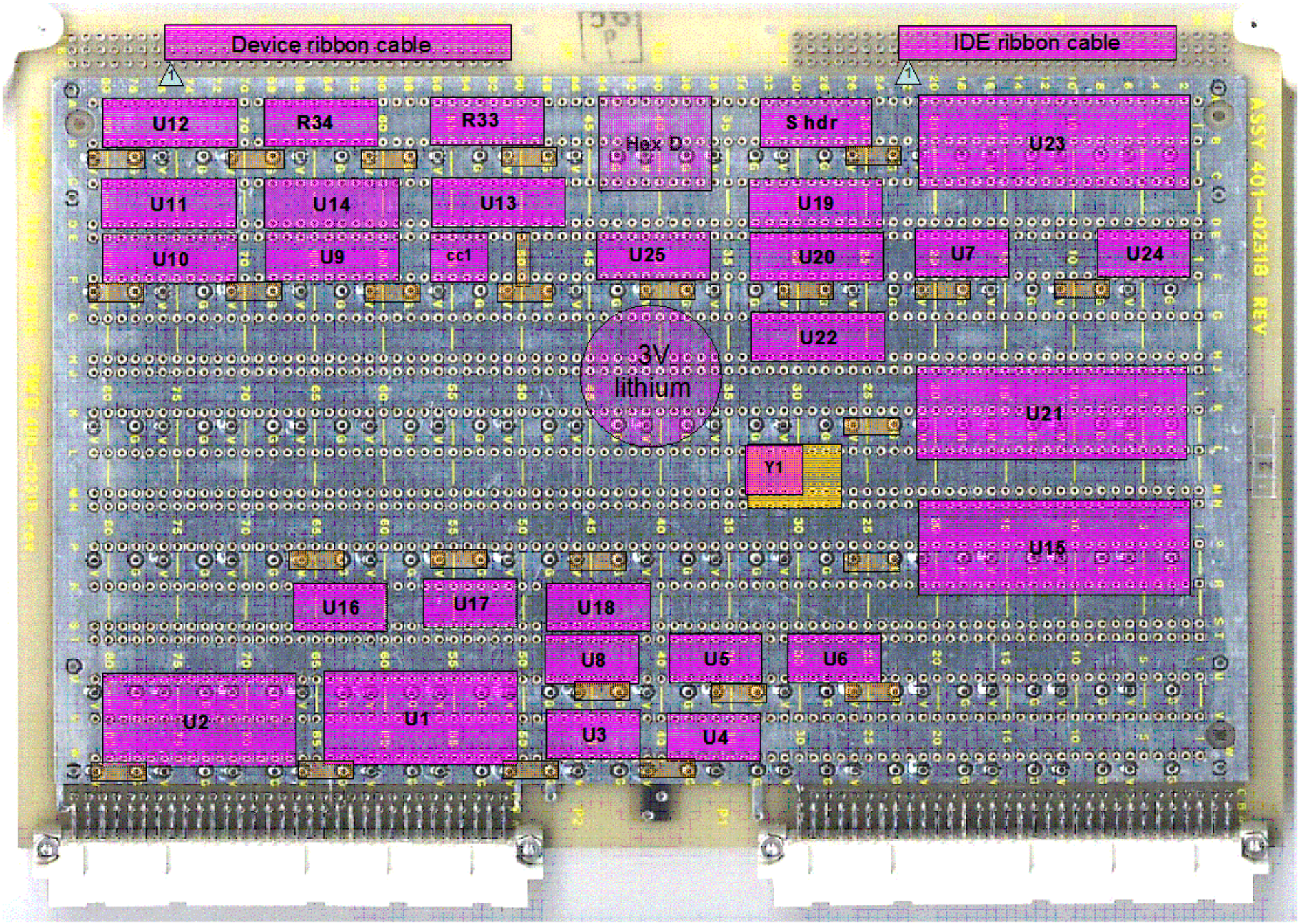
SRAM



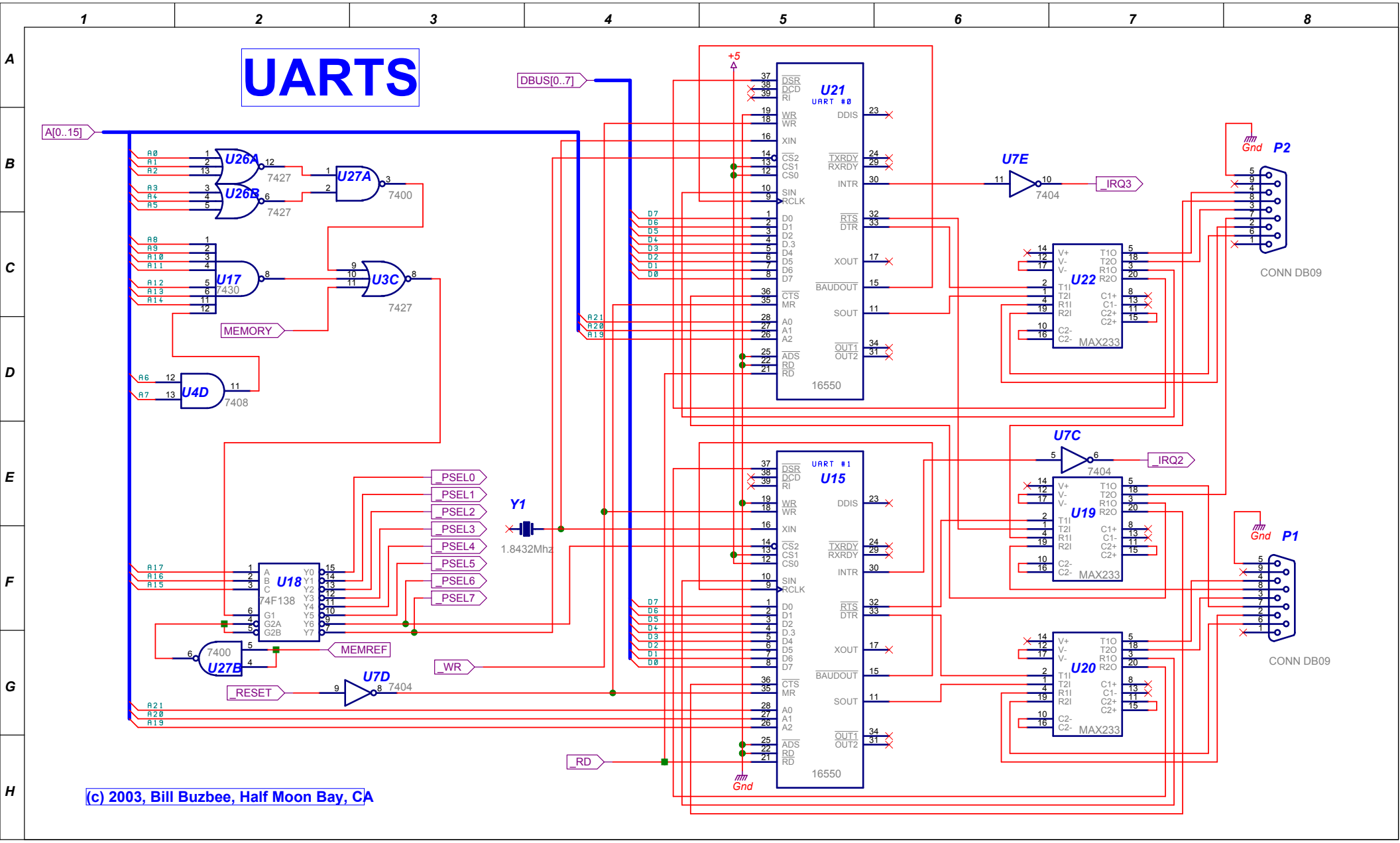
Bill of materials -- Memory Card --- page 1

Item	Qty	References	Value
1	1	U19	7400
2	1	U13	7402
3	1	U11	7404
4	3	U14,U15,U16	7408
5	1	U18	7410
6	1	U20	7420
7	1	U17	7427
8	1	U30	7432
9	4	U7,U8,U9,U10	74157
10	1	U12	74273
11	1	U29	74F138
12	4	U3,U4,U5,U6	74F374
13	8	U21,U22,U23,U24,U25,U26,U27,U28	BIGSRAM
14	2	U1,U2	FAST_SRAM

Device Card



cc1 -> component carrier for D20, D21, R35


UARTS
DBUS[0..7]
A[0..15]
U26A
7427
U26B
7427
U27A
7400
U17
7430
U3C
7427
MEMORY
U4D
7408
U18
74F138
_PSEL0
_PSEL1
_PSEL2
_PSEL3
_PSEL4
_PSEL5
_PSEL6
_PSEL7
Y1
1.8432Mhz
U27B
7400
MEMREF
_WR
U7D
7404
_RESET
_RD
U21
UART #0
U15
UART #1
16550
U7E
7404
_IRQ3
U7C
7404
_IRQ2
U22
MAX233
U19
MAX233
U20
MAX233
P2
P1
CONN DB09
CONN DB09
Gnd
+5
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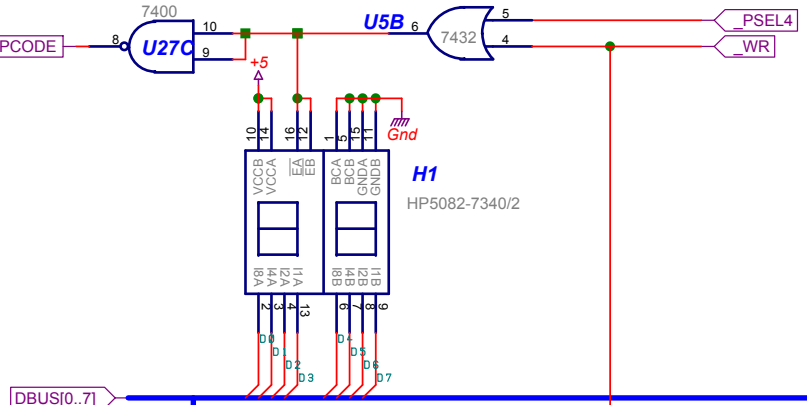
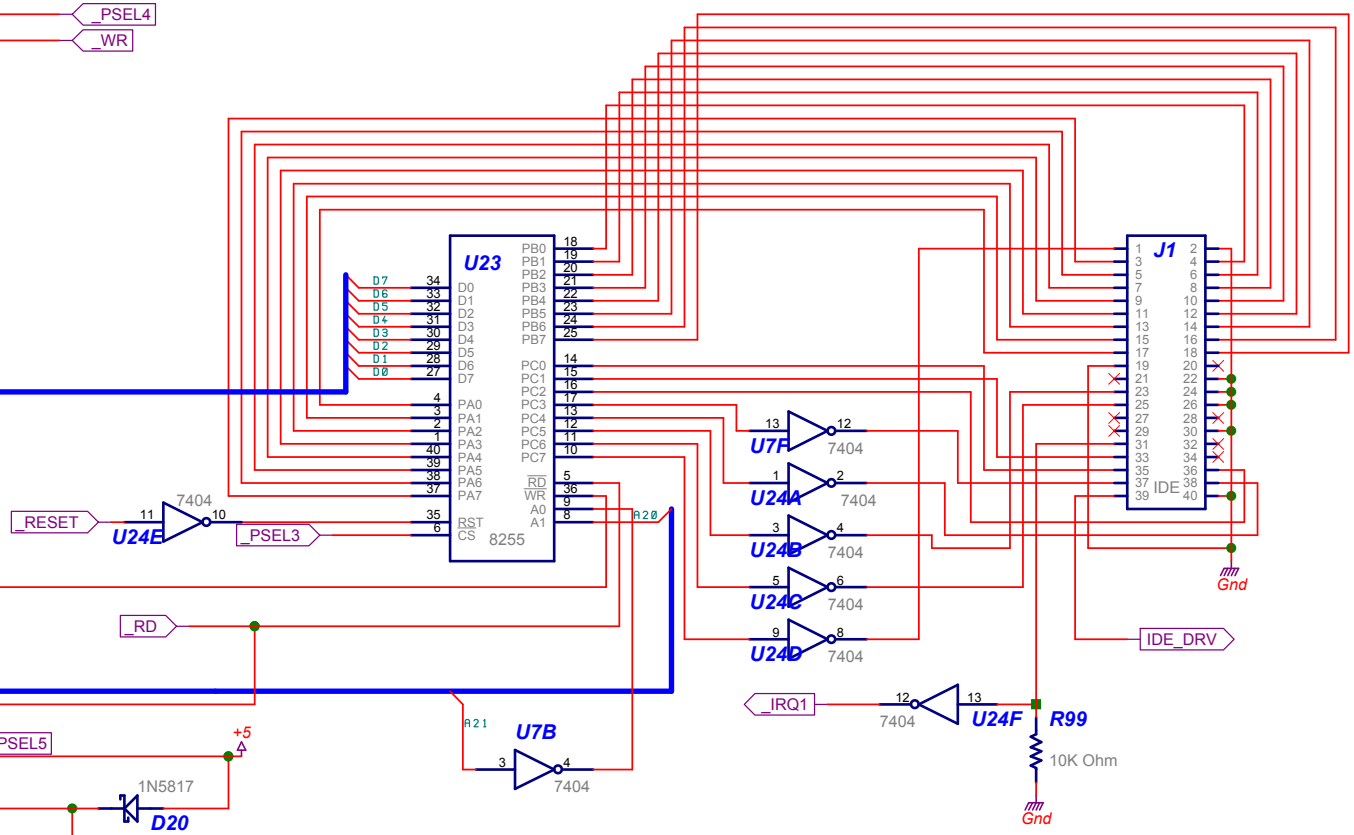
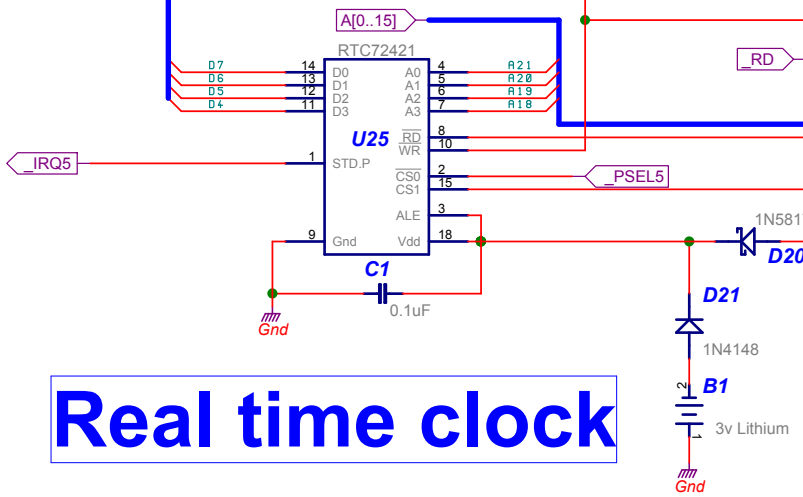
POST Display



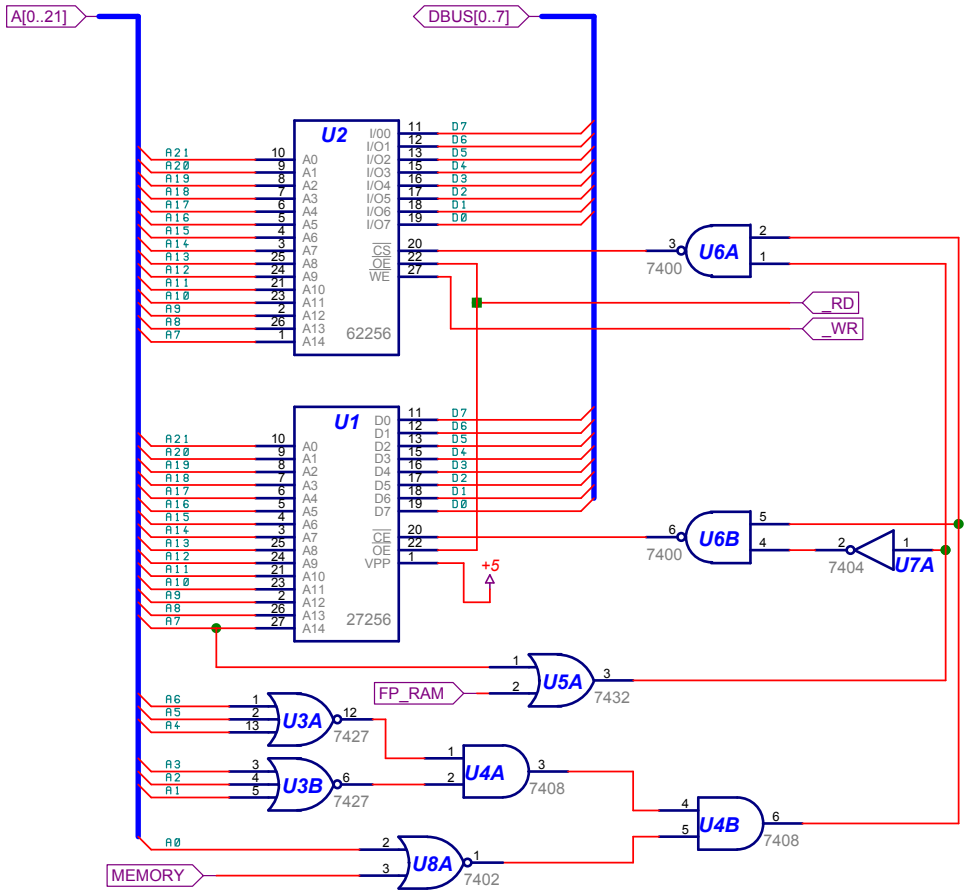
IDE Interface

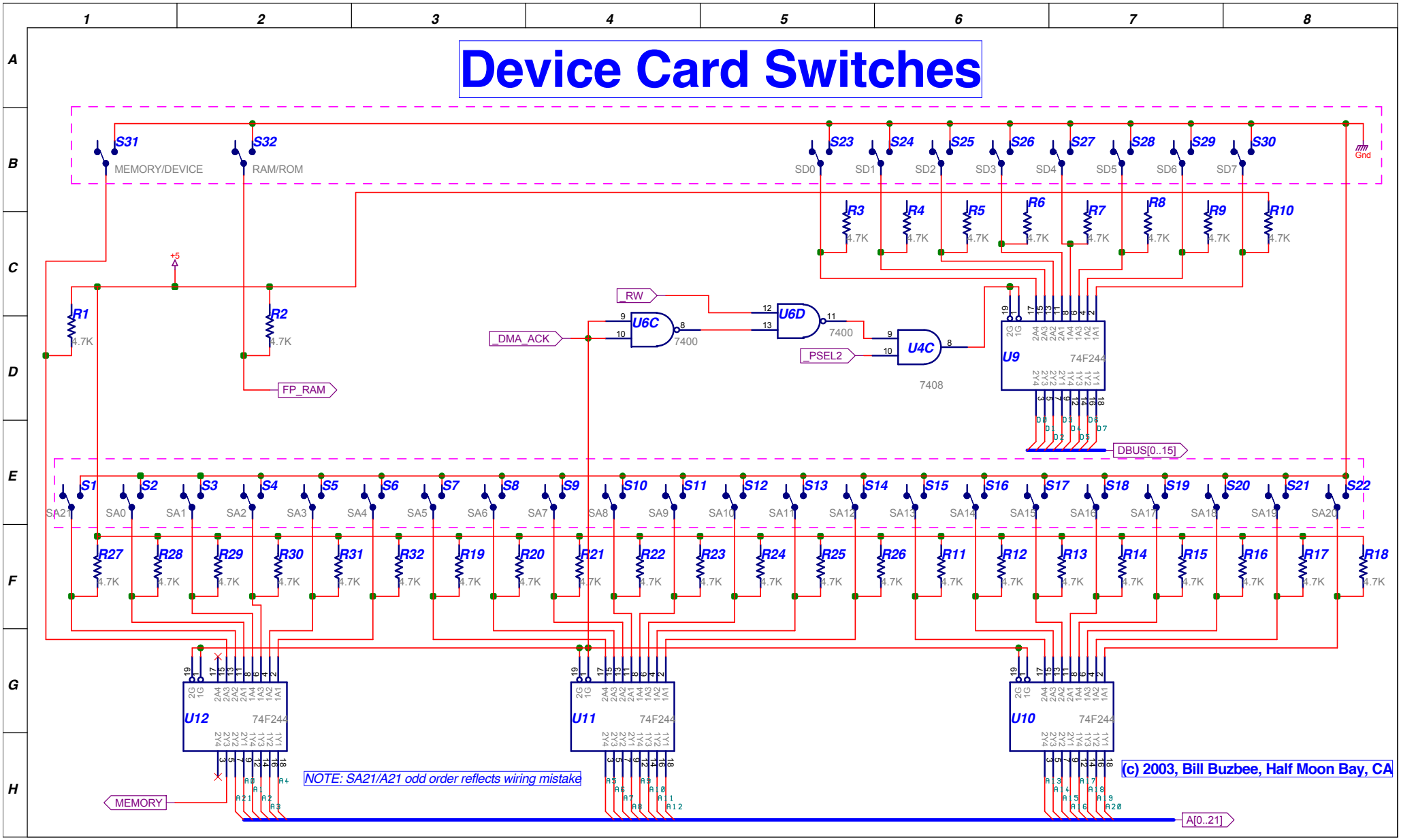


Real time clock



RAM & ROM




Device Card Switches
S31
S32
MEMORY/DEVICE
RAM/ROM
S23
S24
S25
S26
S27
S28
S29
S30
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
Gnd
R3
R4
R5
R6
R7
R8
R9
R10
4.7K
+5
R1
R2
FP_RAM
_RW
_DMA_ACK
U6C
U6D
U4C
7400
7408
_PSEL2
U9
74F244
DBUS[0..15]
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
SA21
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
SA17
SA18
SA19
SA20
R27
R28
R29
R30
R31
R32
R19
R20
R21
R22
R23
R24
R25
R26
R11
R12
R13
R14
R15
R16
R17
R18
U12
U11
U10
NOTE: SA21/A21 odd order reflects wiring mistake
MEMORY
A[0..21]
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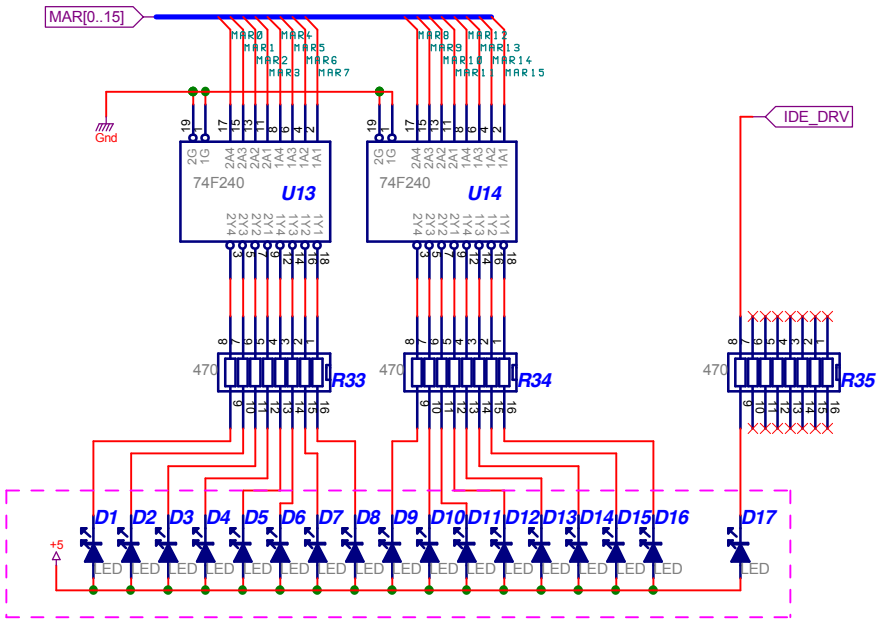
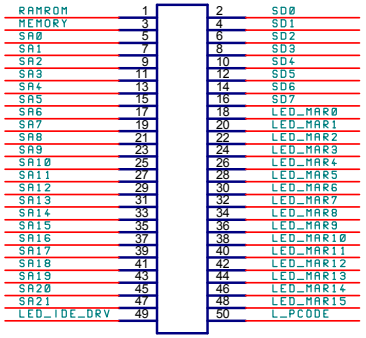
Device LED



Device Ribbon Cable

Right

W1



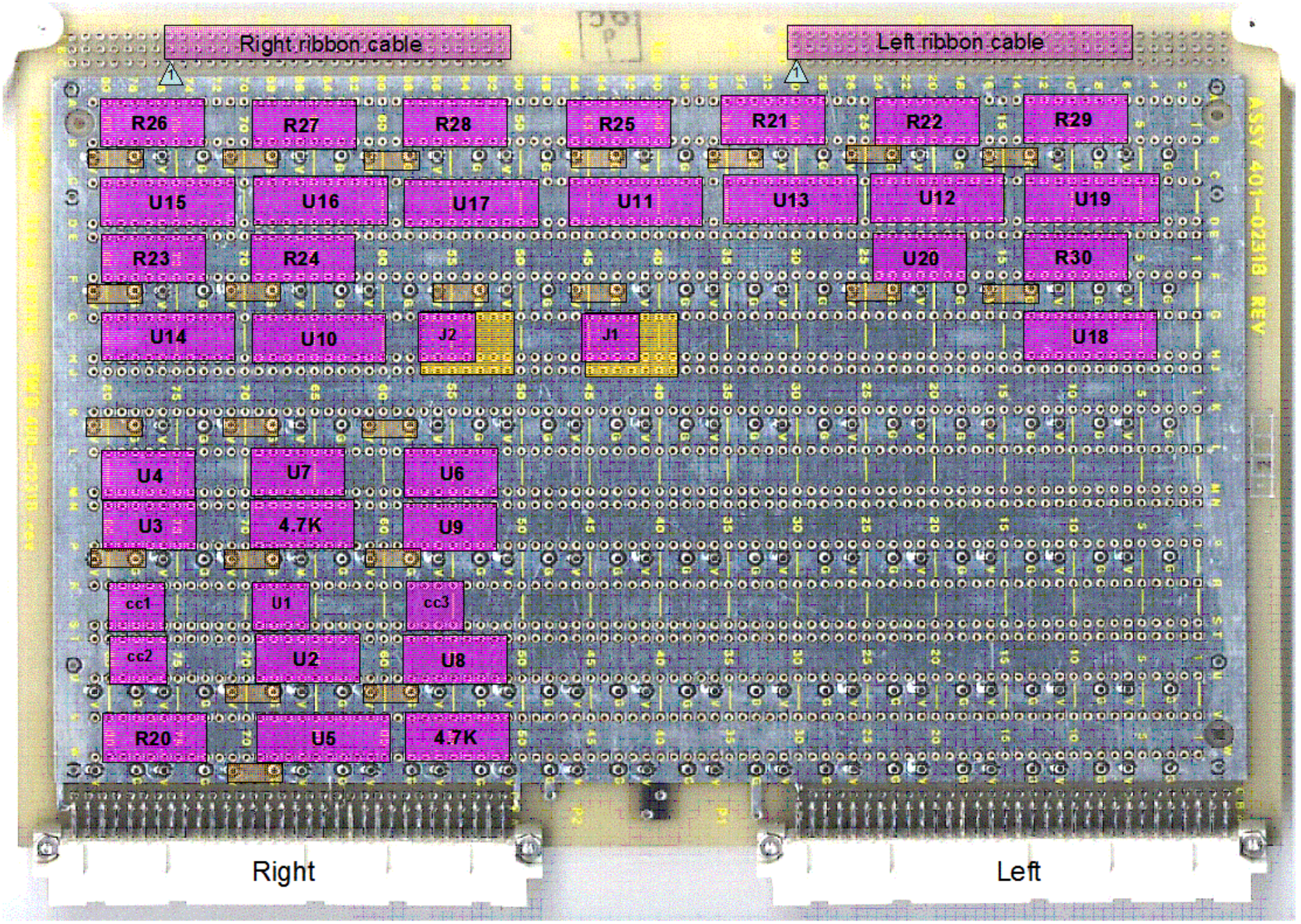
Ribbon50

Device BOM

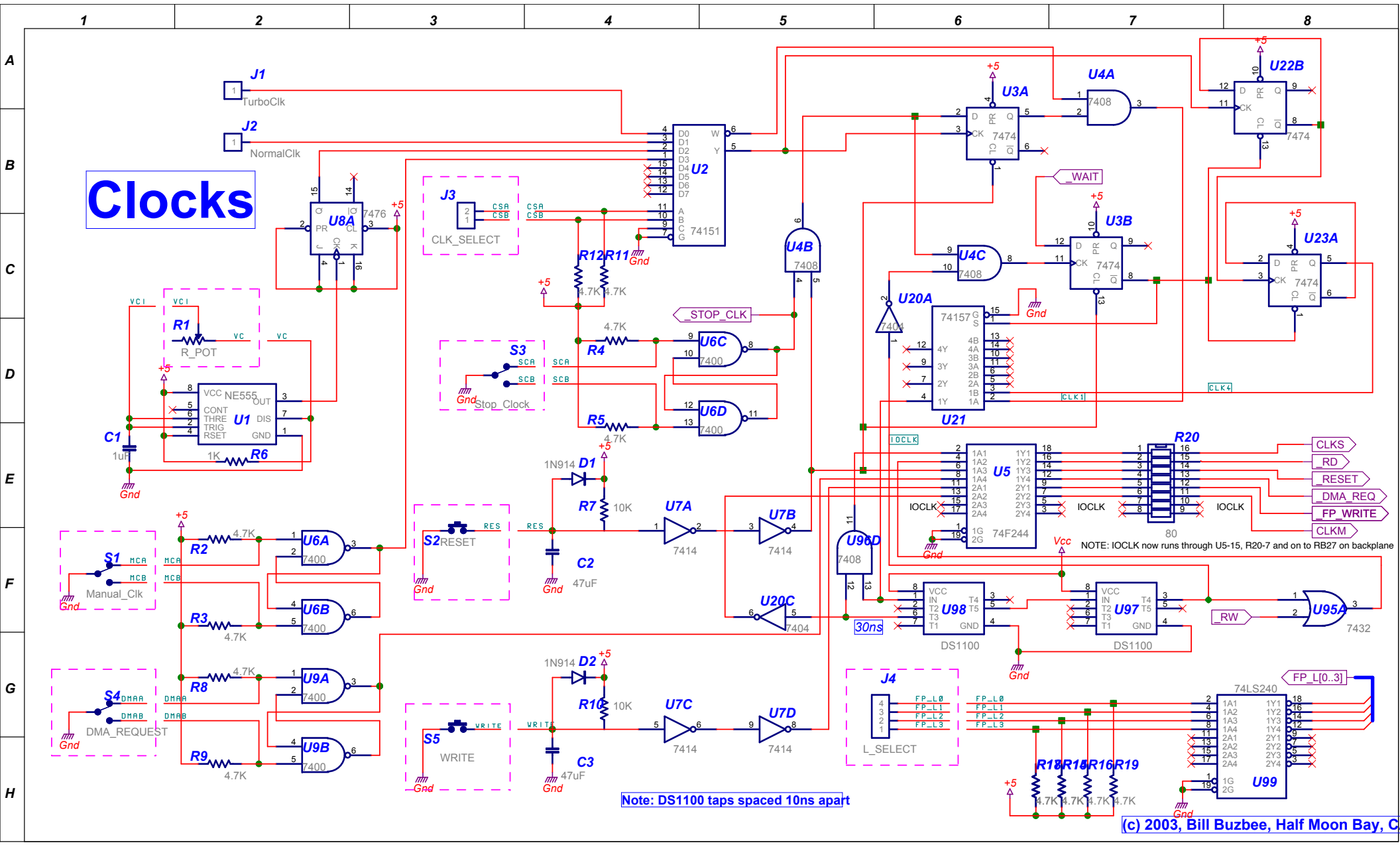
Item	Qty	References	Value
1	3	R33,R34,R35	470
2	1	J1	IDE
3	17	D1,D2,D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13, D14,D15,D16,D17	LED
4	1	S2	SA1
5	1	S3	SA2
6	1	S4	SA3
7	1	S5	SA4
8	1	S6	SA5
9	1	S7	SA6
10	1	S8	SA7
11	1	S9	SA8
12	1	S10	SA9
13	1	S1	SAO
14	1	S23	SD0
15	1	S24	SD1
16	1	S25	SD2
17	1	S26	SD3
18	1	S27	SD4
19	1	S28	SD5
20	1	S29	SD6
21	1	S30	SD7
22	32	R1,R2,R3,R4,R5,R6,R7,R8,R9,R10,R11,R12,R13, R14,R15,R16,R17,R18,R19,R20,R21,R22,R23,R24, R25,R26,R27,R28,R29,R30,R31,R32	4.7K
23	2	U6,U27	7400
24	1	U8	7402
25	2	U7,U24	7404
26	1	U4	7408
27	1	U3,U26	7427
28	2	U16,U17	7430
29	1	U5	7432
30	1	U23	8255
31	1	S12	SA11
32	1	S13	SA12
33	1	S14	SA13
34	1	S15	SA14
35	1	S16	SA15
36	1	S17	SA16
37	1	S18	SA17
38	1	S19	SA18
39	1	S20	SA19
40	1	S11	SA1O
41	1	S21	SA20
42	1	S22	SA21
43	1	C1	0.1uF
44	2	U15,U21	16550
45	1	U1	27256
46	1	U2	62256
47	1	D21	1N4148
48	1	D20	1N5817
49	1	U18	74F138
50	2	U13,U14	74F240
51	4	U9,U10,U11,U12	74F244
52	3	U19,U20,U22	MAX233
53	2	D18,D19	TIL311
54	1	S32	RAM/ROM
55	1	W1	Ribbon50
56	1	U25	RTC72421
57	1	Y1	1.8432Mhz

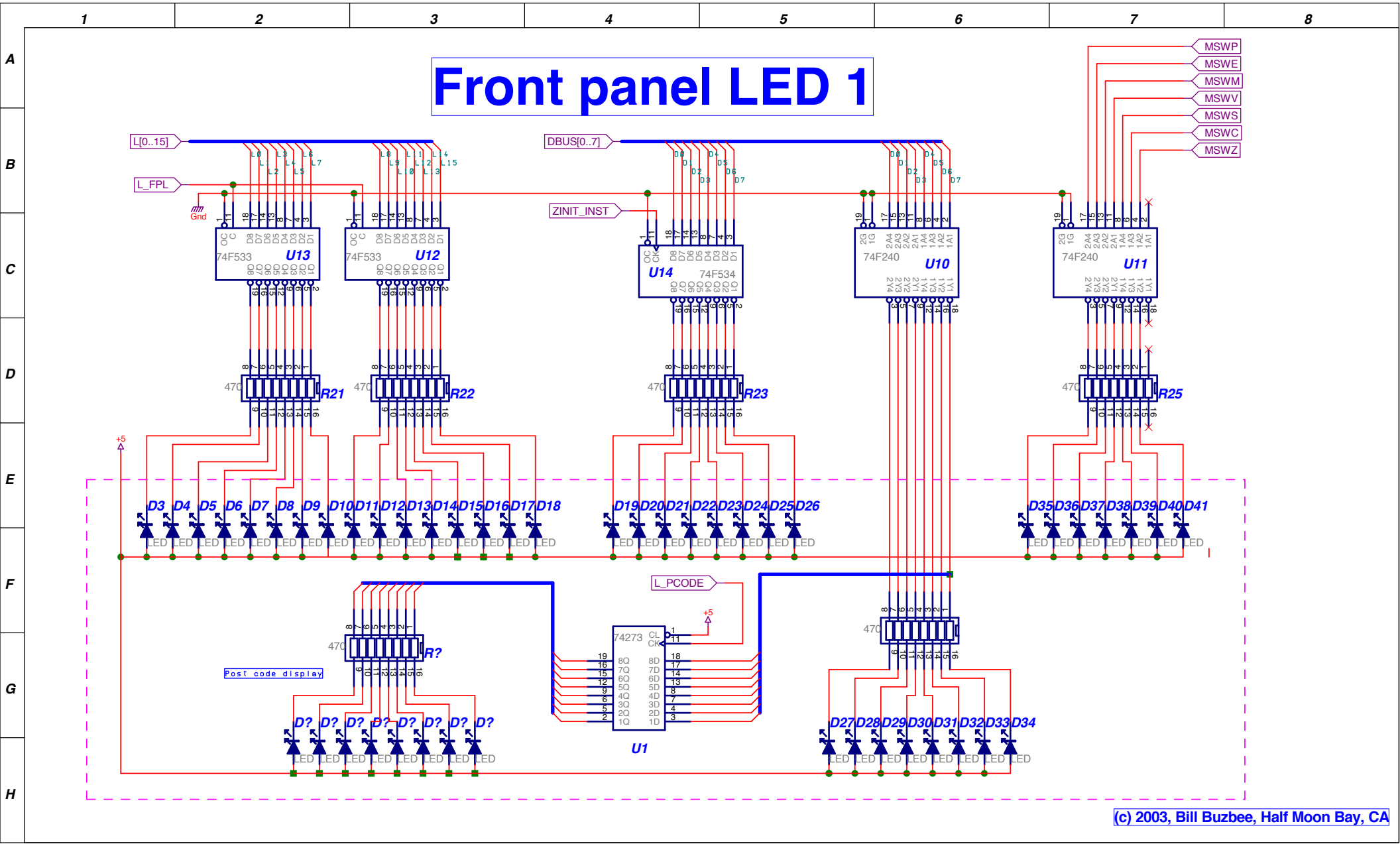
58	2	P1,P2	CONN DB09
59	1	B1	3v Lithium
60	1	S31	MEMORY/DEVICE

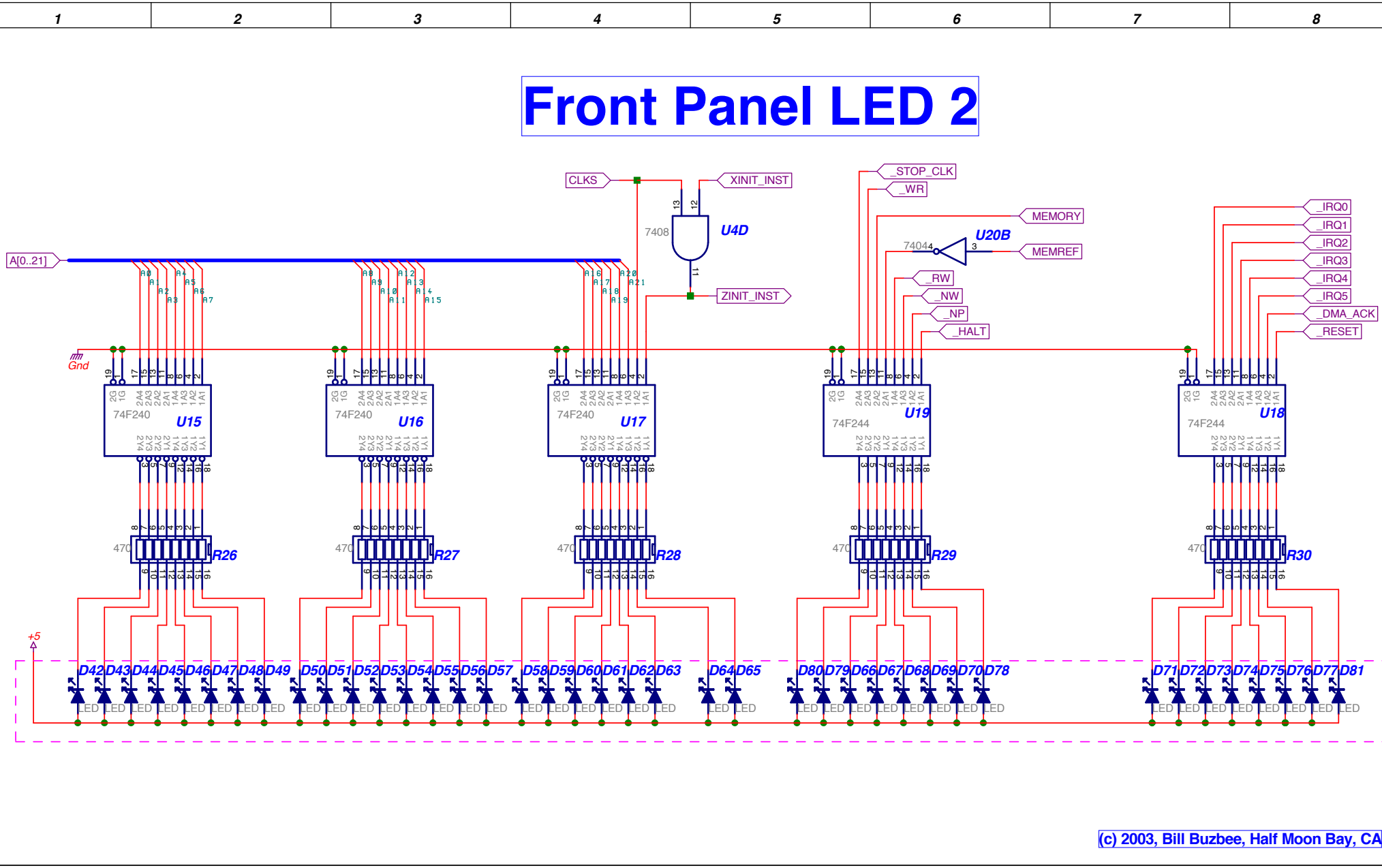
Front Panel Card



cc1 -> component carrier for _FP_WRITE
cc2 -> component carrier for _RESET
cc3 -> component carrier for 555 circuit


Clocks
J1
TurboClk
J2
NormalClk
U2
74151
J3
CLK_SELECT
CSA
CSB
U8A
7476
R12
R11
4.7K
Gnd
+5
U4B
7408
_STOP_CLK
U6C
7400
U6D
7400
R4
R5
S3
Stop_Clock
SCA
SCB
R1
R_POT
VC
VCI
C1
1uF
U1
NE555
R6
1K
D1
1N914
R7
10K
U7A
7414
U7B
7414
S2
RESET
RES
C2
47uF
U20C
7404
U96D
7408
U3A
7474
U4A
7408
U22B
7474
_WAIT
U3B
7474
U4C
7408
U20A
7404
U23A
7474
74157
U21
IOCLK
U5
74F244
R20
80
CLKS
_RD
_RESET
_DMA_REQ
_FP_WRITE
CLKM
NOTE: IOCLK now runs through U5-15, R20-7 and on to RB27 on backplane
Vcc
U98
DS1100
U97
DS1100
30ns
_RW
U95A
7432
S1
Manual_Clk
MCA
MCB
R2
R3
U6A
U6B
7400
S4
DMA_REQUEST
DMAA
DMAB
R8
R9
U9A
U9B
7400
S5
WRITE
D2
R10
C3
U7C
U7D
7414
J4
L_SELECT
FP_L0
FP_L1
FP_L2
FP_L3
74LS240
FP_L[0..3]
R18
R17
R16
R19
U99
Note: DS1100 taps spaced 10ns apart
(c) 2003, Bill Buzbee, Half Moon Bay, C

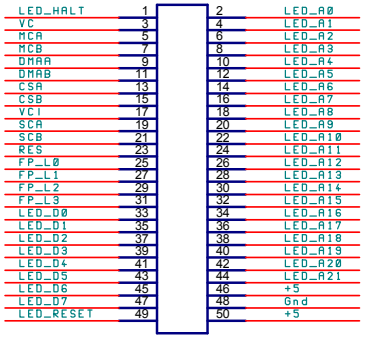

Front panel LED 1
L[0..15]
L_FPL
Gnd
DBUS[0..7]
ZINIT_INST
MSWP
MSWE
MSWM
MSWV
MSWS
MSWC
MSWZ
74F533
U13
U12
U14
74F534
74F240
U10
U11
R21
R22
R23
R25
+5
D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18
D19 D20 D21 D22 D23 D24 D25 D26
D35 D36 D37 D38 D39 D40 D41
L_PCODE
74273
U1
R?
Post code display
D? D? D? D? D? D? D? D?
D27 D28 D29 D30 D31 D32 D33 D34
LED
(c) 2003, Bill Buzbee, Half Moon Bay, CA


Front Panel LED 2
CLKS
XINIT_INST
7408
U4D
ZINIT_INST
_STOP_CLK
_WR
MEMORY
7404
U20B
MEMREF
_RW
_NW
_NP
_HALT
_IRQ0
_IRQ1
_IRQ2
_IRQ3
_IRQ4
_IRQ5
_DMA_ACK
_RESET
A[0..21]
Gnd
74F240
U15
U16
U17
74F244
U19
U18
R26
R27
R28
R29
R30
+5
D42 D43 D44 D45 D46 D47 D48 D49
D50 D51 D52 D53 D54 D55 D56 D57
D58 D59 D60 D61 D62 D63
D64 D65
D80 D79 D66 D67 D68 D69 D70 D78
D71 D72 D73 D74 D75 D76 D77 D81
LED
(c) 2003, Bill Buzbee, Half Moon Bay, CA

Front Panel Ribbon Cable

Right

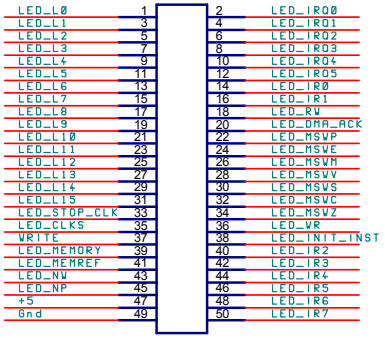
W1



Ribbon50

Left

W2



Ribbon50

Front Panel BOM

Item	Qty	References	Value
1	2	C2,C3	C
2	1	R6	1K
3	1	R20	80
4	1	C1	.01
5	10	R21,R22,R23,R24,R25,R26,R27,R28,R29,R30	470
6	78	D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,D15, D16,D17,D18,D19,D20,D21,D22,D23,D24,D25,D26, D27,D28,D29,D30,D31,D32,D33,D34,D35,D36,D37, D38,D39,D40,D41,D42,D43,D44,D45,D46,D47,D48, D49,D50,D51,D52,D53,D54,D55,D56,D57,D58,D59, D60,D61,D62,D63,D64,D65,D66,D67,D68,D69,D70, D71,D72,D73,D74,D75,D76,D77,D78,D79,D80	LED
7	17	R2,R3,R4,R5,R7,R8,R9,R10,R11,R12,R13,R14,R15, R16,R17,R18,R19	4.7K
8	2	U6,U9	7400
9	1	U20	7404
10	1	U4	7408
11	1	U7	7414
12	1	U3	7474
13	1	U8	7476
14	2	D1,D2	1N914
15	1	U2	74151
16	1	U1	NE555
17	1	R1	R_POT
18	1	S2	RESET
19	1	S5	WRITE
20	5	U10,U11,U15,U16,U17	74F240
21	3	U5,U18,U19	74F244
22	2	U12,U13	74F533
23	1	U14	74F534
24	1	J4	L_SELECT
25	2	W1,W2	Ribbon50
26	1	J1	TurboClk
27	1	J2	NormalClk
28	1	S1	Manual_Clk
29	1	S3	Stop_Clock
30	1	S4	DMA_REQUEST
31	1	J3	CLOCK_SELECT